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Real Implementation of Arm 9 Processor Based Digital Private Branch Exchange

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Abstract: PBX (Private Branch Exchange) is introduced for providing internal calls without cost. In the beginning, analog PBX is developed for internal communication. It has low voice and cross talk errors. Those errors were eliminated by developing digital PBX using Pentium-I processor CPU board. It shows results in much product cost, larger in size and demand for Pentium processors (Obsolete model) also increased rapidly in these days. In this study, implement a digital PBX system CPU using 32-bit ARM 9 processor (S3C2440) which is a compact and cost effective design when compared existing system. A PBX is mainly used in companies, hotel and private complexes.

Key words: S3C2440A, digital cross point switch (MT8980), DTMF receiver (MT8870), CPU board, India

INTRODUCTION

Now-a-days, telecommunication is very important for our business world. Any business needs internal telecommunication without call cost. Depending on the business, telephone connection may differ. If the business is small, must have at least two lines, one for telephone calls and the other for use with a facsimile machine. When more than 2 lines are needed, it needs a PBX system for providing extension lines and call routing purpose. Advanced PBX system offer features like voice mail, auto-call attendant, DID (Direct Inward Dialling), etc.

Kasson (1979) is described about the computerized branch exchange operation and their functions. In this computerized branch exchange, uses Time Division Multiplexing (TDM) with Pulse Code Modulation (PCM) for digital bus. In digital switching section, each exchange PCM coded voice information should be collected in TSI (Time Slot Interchange). This information is stored into a small time interval and arrange multiple slots on a common transmission bus to constitute a continuous frame. Mischar Schwartz introduced concept of TSI, uses buffered memories and also it provides time/space switch functionality. Du Toit (1992) presents cost effective PBX communication system features. Win (2008) create a model PBX system using low cost micro-controller. DTMF receiver working function described by Ekinci and Atalar (1995). Digit receiving from phone by using DTMF receiver and send caller-id to phone by using DTMF transmitter described by Shatnawi *et al.* (1997). Shen and Hwang (2009) was proposed new algorithm for DTMF digit detection.

In the 21st century, most embedded integrated industrial control systems based on ARM structure. ARM chips boast strong performance besides compact size and low power consumption. ARM 7 supports frequency up to 60 MHz but in ARM 9 core supports frequency up to 400 MHz; high level implementation of the 5-stage pipelined ARM9 core represented by Arandilla *et al.* (2010). Segars (1998) explained comparison with the ARM7TDM, ARM9 core consumed 72% more average power and occupied 63% larger chip size. This is largely due to the increase in the number of registers in the control unit and additional blocks needed to support the 5-stage pipeline and the Harvard architecture. The S3C2440A consists of a 32-bit ARM920T RISC core which implements the AMBA bus and Harvard cache architecture. Main features of S3C2440A, it required less power supply voltages compared to ARM microprocessor made by another manufacturer. The minimum power supply needs of its core is 1.3 and 3.3 V for the peripherals like memory interface and external GPIO. The operating speed for the core of S3C2440A is linear to its core voltage rating. The S3C2440 CPU hardware core design for printed circuit board was explained by Sulaiman *et al.* (2011).

PBX SYSTEM ARCHITECTURE

DPBX adopts digital time/space switching technology to provide inter-communication. This system is modular and expandable in nature. It supports 200 (64 k bits sec^{-1}) channels which can be increased to 256 (64 k bits sec^{-1}) channels. S3C2440A processor has the two types of flash memories as: NAND flash and NOR

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flash. Digital PBX needs frequency range up to 400 MHz. The programming code should be stored in the NAND flash memory.

Figure 1 shows PBX system architecture. The system architecture is such that a terminal group can handle a maximum of 8 extension ports. Each terminal group facilitates time division multiplexing of 32 channels at 64 kbps. So, this would generate a PCM stream with a bit rate of 2.048 Mbps from each terminal group. In this fashion, the architecture is designed to handle a maximum of 8 terminal groups.

All terminations (Extensions, trunks) interface with switching network which is controlled by ARM 9 processor. The extensions are terminated in the Line Card (LCC) and the trunk lines in the Trunk card (TRK). Tone and Sync card generates the various tones and synchronization signals necessary for exchange operation. DTMF card supports DTMF dialer. PCM stream from termination are interfaced with digital cross point CPU card residing in the main CPU module. Main CPU (Based on ARM 9) receives the PCM stream from digital cross point CPU card. The Tone and Sync card generates the synchronization signals which can be fed to the various cards. The digital cross point CPU controlled by the ARM 9 family processor. The power supply for the whole system is derived from 230Vac which is converted to necessary AC and DC voltages by a PSU and SMPS module. All the signalling information of various terminations and junction cards are multiplexed with their PCM stream.

Terminal group consists of 8-Line card, 3-Trunk card, 1-Tone and Sync card and 2-DTMF card. These cards are housed in a 13 slot card frame. Necessary inter-connections between the cards are achieved through mother board. Between the termination modules, the connection is through cable. Each line card interfaces 16 extensions with DPBX. In this system, 18-Line cards supports 128 extensions. Analog to digital conversion of each junction incoming/outgoing voice signals is done by PCM codec. The digital output signal is multiplexed with the main stream which is sent to the digital cross point card at the rate of 2.048 Mbps. Also, the signalling information about extensions is processed in a similar way and the digitized output is multiplexed with the main stream. Each trunk card interfaces 8 trunks with DPBX. In this system, 3-Trunk cards supports 24 junctions. Analog to digital conversion of each junction incoming/outgoing voice signals is done by PCM codec. The digital output signal is multiplexed with the main stream which is sent to the digital cross point card at the rate of 2.048 Mbps. Also, the signalling information about extensions is processed in a similar way and the digitized output is multiplexed with the main stream.

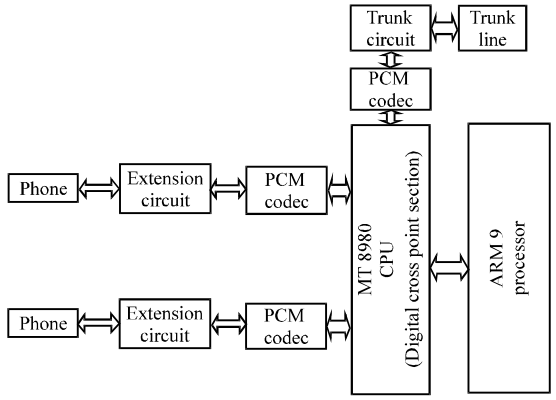

Fig. 1: PBX system architecture

Scanning and switching on extension and trunk lines done by DXPT card. Dialer card provides Caller ID. Trunk card has inbuilt dialler section and extension card has separate dialler section. In this system, process scanning every extension port within 11 m sec once via DXPT card, if presence of line detection in any extension line that show off hook state of the phone. When the idle state of extension, switch the dial tone and DTMF to the particular extension. If that extension line dialled any digit, check whether a valid extension number via DTMF card if the valid tone present, provide ringing and send caller ID for that extension. If ringing extension coming into the off hook state, provide a speech path for two extensions via DXPT card. After any one of the extension is on hook state, disconnect speech path among two extensions and send call details to PC via serial port at 115200 baud rate. If dialled digit in an extension as trunk fetching code, switch trunk line into extension line and scanning dialled digits into trunk line. If the extension line goes to on hook state, disconnect the trunk line from the extension line and provides call details with duration for accounting purposes.

DIGITAL CROSS POINT SECTION (DXPT)

DXPT card connects with ARM 9 processor GPIO ports and interfaces with exchange for switching the digitized voice signal. The heart of the card is MT8980 digital time/space cross point switch which can support maximum 256 ports (non-blocking) switching. The exchange generates an incoming serial PCM stream Sti0-Sti7 which is fed to the DXPT card through flat cables. In the DXPT card, those input streams are fed into MT8980 through buffering chips. Similarly DXPT generates outgoing switched PCM stream Sto0-Sto7 which is buffered through 74HC244 and then fed to the

exchange. For the internal processing, this card interfaces with ARM 9 Processor. The Data lines (D0-D7) and Address lines (A0-A15) are buffered bidirectional through the transceiver which is fed to the EPROM and MT8980.

Main switching of the received serial PCM Sti is done in accordance with address selected in MT8980 by Address lines (A0-A5). The necessary control signals such as R/W (Read/Write), DS (Data Strobe), CS (Chip Select) and DTA (Data Acknowledge) must be present. The clock signals C4i, F0i are also fed to MT8980. The switched output in the form of serial PCM Stream output (Sto). The main program is stored in the EPROM. This program is executed by the ARM 9 processor.

Channels are referenced to the start of the frame and are numbered from 0-31. The clock input of the MT8980 is called C4i and its frequency (4.096 MHz) is twice the data rate. There are three types of memory as: Connection memory high, connection memory low and data memory. A5 control register is used to select the memory. Further address lines are used to indicate (0-31) channel number. By selecting a switching mode and message mode by connection memory high and connection memory low.

In existing system DXPT card with Pentium-I CPU shown in Fig. 2. Single MT8980 chip makes connection (8 input and 8 output pins) 256×256 possible connection, hardware connection for single chip as shown in Fig. 3. Read/write and data strobe signal is connected to the Pentium-I CPU ISA (International Standard Architecture) slot Read (IOR) and Write (IOW) signals as shown in Fig. 4. When IOW signal is low, write operation of MT8980 is selected and data strobe is high. When IOR signal is low, read operation of MT8980 is selected and data strobe should be high. DTA (Data Acknowledgement) signal and chip select of MT8980 is given to the IO/CH ready of Pentium-I ISA slot pin. During the reading and writing operation of MT8980 CPU, IO/CH ready is waiting for their completion of operation via DTA signal. But, in this new S3C2440A based CPU, IO/CH ready pin is not available. For that, data acknowledgement read the DTA pin via GPIO port.

Four MT8980 chip arranged for non-blocking switching block diagram as shown in Fig. 5. Figure 6 shows hardware implementation of non-blocking switch section. In this, hardware has 16 input and 16 output pins, make 512×512 possible connection can always reach an available line without encountering a busy condition. In

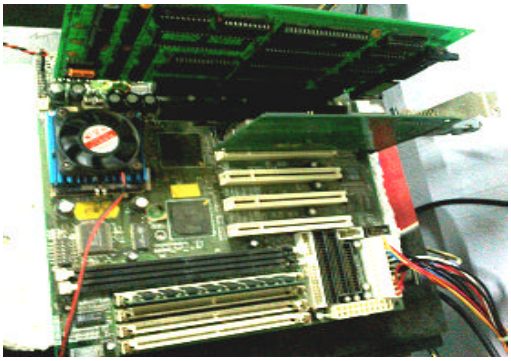

Fig. 2: DXPT card with Pentium-I CPU

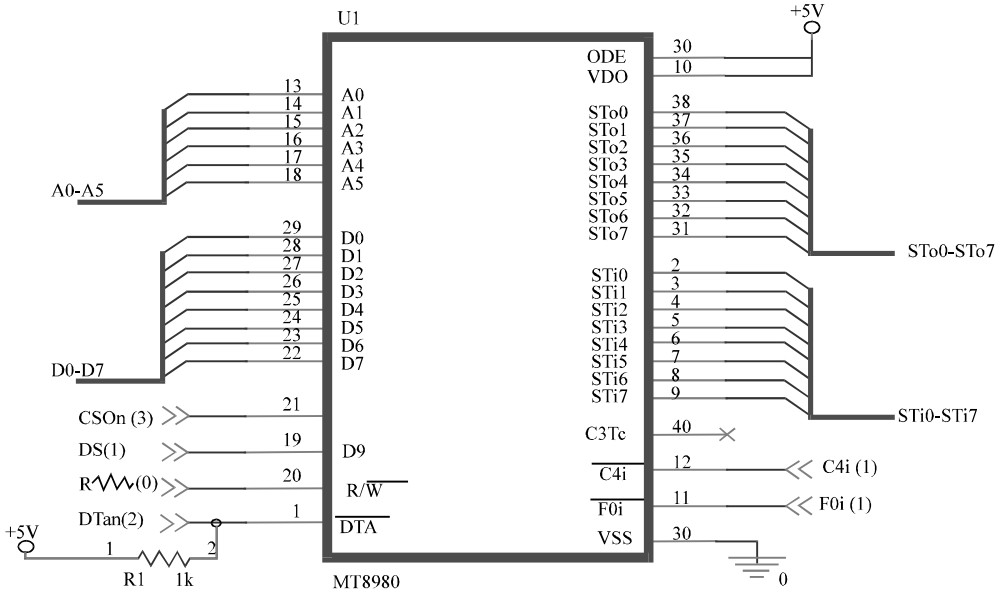

Fig. 3: Single MT8980 connection

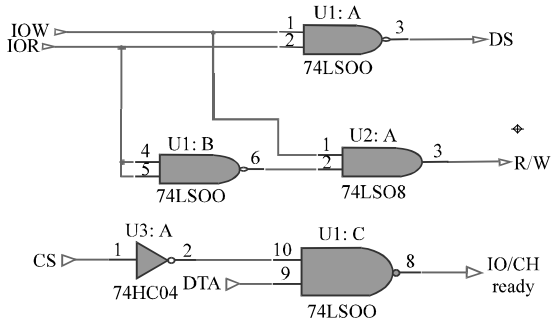

Fig. 4: IOR, IOW, IO/CH ready

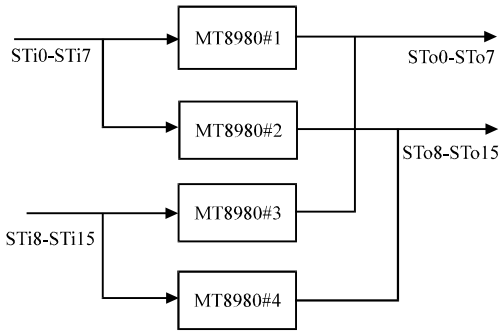

Fig. 5: Non-blocking switching

Fig. 6: DXPT card

first 256 possible connection used for switching extension speech connection. Another 256 connection is used for scanning extension line and extension ring driving purposed.

Figure 6 shows image of DXPT card. For storing extension features like call forward, call follow me will be stored in EEPROM (2 Kbits). ARM 9 processor based CPU system setup shown in Fig. 7, it consists of ARM 9 development board and DXPT card and clock section.

In power up condition (Fig. 8a), each stream output will be any value. At initialization set as all stream output as high impedance state by writing 1's to the all stream and channel. That state is called as Idle state as shown in Fig. 8b. When switching 1st stream 5th channel input into 1st stream output all channels were done in software.

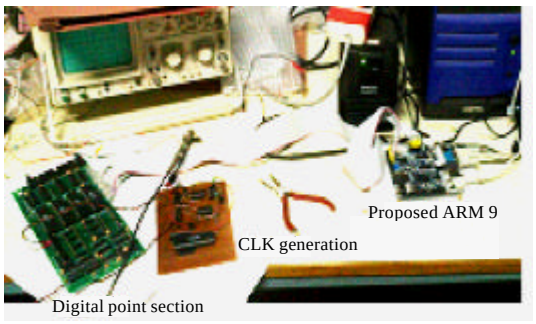

Fig. 7: ARM 9 based CPU communicates with DXPT card

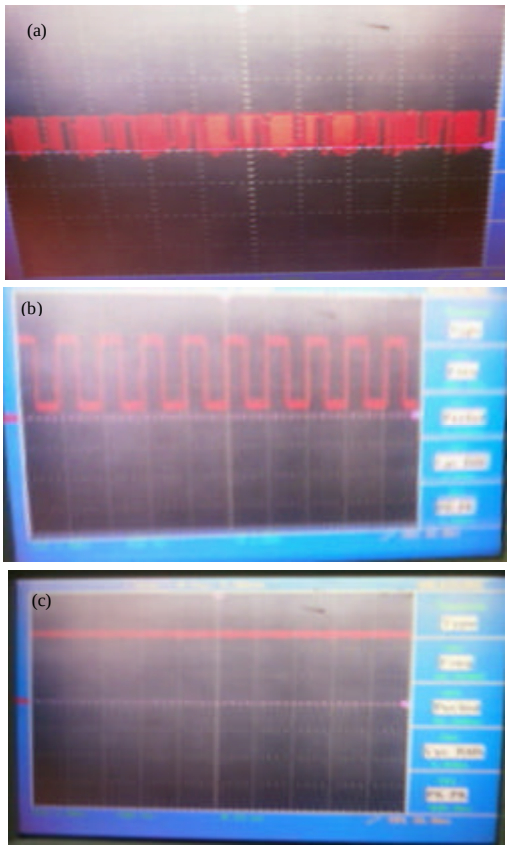

Fig. 8: a) ST-BUS at power up condition; b) ST-BUS output idle state; c) ST-BUS output when switching 1m sec pulse in ST-BUS input

If 1 m sec pulse input was given to the 1st stream 5th channel stream input, output pin 1st stream has shown in Fig. 8c.

CONCLUSION

Pentium-I based digital PBX CPU is replaced with 32-bit ARM 9 (S3C2440A) processor. When this

S3C2440A based CPU, it supports >200 extension ports and 20 trunk lines. The MT8980 card is successfully interfaced with S3C2440, comparing the existing system which inherits less cost, small die size and low power consumption. If any fault occurs like software corruption in S3C2440A, it can reprogrammed in NAND flash memory via USB or JTAG dongle or replace the MICROS3C2440 chipset with another working MICROS3C2440 chip set. S3C2440A CPU also has the connectivity of Ethernet, VGA monitor, memory card for storing call details and not required additional PC connection.

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