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Performance Analysis of 6-Transistor Full Adder Circuit using PTM 32 nm Technology LP-MOSFETs and DG-FinFETs

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Abstract: Power consumption and speed are two primary design constraints for Integrated Circuits (ICs). Improved performance on the basis of these is achieved primarily by reducing the silicon area of the IC. With reduced number of transistors to design a Full Adder (FA) circuit, high speed, low power Arithmetic Logic Units (ALUs) can be built which is a fundamental component of digital circuit. In this study, a performance analysis of a recently proposed 6-Transistor (6T) FA circuit has been presented using 32 nm Predictive Technology Models (PTM). Comparative analysis has been carried out between Low Power (LP) MOSFET and Double-Gate (DG) FinFET in the circuit. The PTM-LP MOSFET proved to be a better device for low power circuit while the DG FinFET proved a better alternative in terms of low chip area, high speed and good output voltage level and uniformity. Performance analysis also showed requirement of passive elements and transistor size modification for desired output with the 6T design.

Key words: Full adder, MOSFET, DG-FinFET, low power, low chip area, high speed

INTRODUCTION

Full adder is one of the core building blocks in different Very Large Scale Integration (VLSI) circuits as well as the basic functional unit of an ALU. In recent days, designing low power and high speed full adders is becoming more popular. The circuit operation and overall capability of the system are affected by large power consumption. Furthermore, it also increases the cost of cooling the VLSI systems.

Over the years, several research groups have proposed different models to design full adder circuits using different logic styles to reduce the overall transistor count and hence, improve power consumption, area and speed performances. Each design technique has its own pros and cons. Along with reduction in transistor number, it is needed to scale down the supply voltage and vary the Width/Length (W/L) ratio of the transistors. A 32 Transistor (32-T) based design used with Complementary Pass-transistor Logic (CPL) exhibits better capability in producing correct output voltages but consumes large amount of power (Zimmermann and Fichtner, 1997). The conventional full adder circuit with pull up and pull-down networks uses 28 transistors with standard Complementary Metal Oxide Semiconductor (CMOS) logic with robustness. The number of transistor was reduced to 26 using a bridge circuit technique which provided better performance with respect to speed and chip area (Navi *et al*., 2008). A review of full adders was presented by Singh *et al*. (2014) using 20T CMOS logic, 15T Transmission Gate (TG) logic and 9T PTL. The 15T TG logic based FA showed the least power requirement and delay. A 12T full adder is proposed by Kumar *et al*. (2012) which used 3T XOR gates and a 2T Multiplexer (MUX). The conventional full adder circuit can be designed using Gate Diffusion Input (GDI) logic to reduce the number of transistors from 28 to only 10 (Morgenshtein *et al*., 2001). Further research has reduced the number of transistors to 8 (Dwivedi and Prakash, 2016) and eventually to a 6T FA (Reddy, 2013; Chandra *et al*., 2015). As the number of transistors reduce, performance is improved in terms of power and speed at the cost of degraded output logic voltage.

In the subject paper, performance analysis of the 6T FA design using traditional MOSFETs and the modern FinFETs with the PTM 32 nm technology models is presented. The following section gives an overview of FinFET. Section III explains the operation of the 6T FA while section IV expounds the different manipulation of parameters and circuit for the simulation and its result. Section V concludes the paper.

FinFET overview: The operational mode of FinFET (Liu, 2012), also known as a multi-gate device is very similar to the conventional MOSFET. The FinFET has a source, a drain and a gate terminal but the channel between the source and drain of FinFET is very different from that of MOSFET. The channel of FinFET is designed on top of the silicon substrate, known as “fin”, as a three-dimensional bar. The gate of FinFET is fully covered around the channel. At nano scale device technology, FinFETs are undertaking alternative to bulk CMOS. The Double-Gate (DG) FinFET gives rise to a rich design space using various configurations of the gates. A major advantage of using FinFET is having better Short Channels Effects (SCEs) performance compared to the conventional CMOS. The structure of a FinFET is shown in Fig. 1.

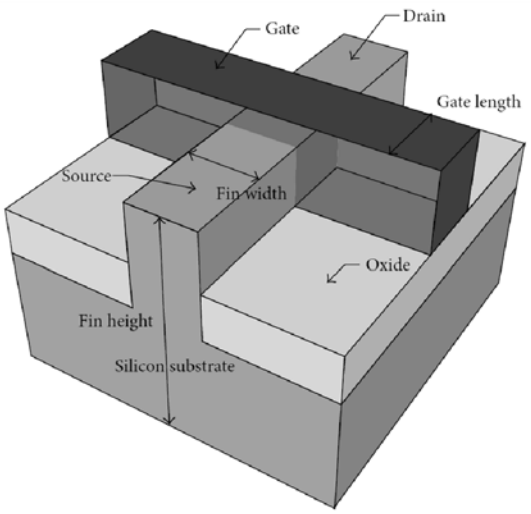

Fig. 1: FinFET structure (Chin *et al*., 2015)

The FinFET has 4 modes of operation: Short-Gate (SG) mode, Independent-Gate (IG) mode, Low-Power (LP) mode and hybrid mode (Priyanka and Patel, 2015).

SG mode: The front gate and the back gate are shorted together for better driving strength. If one of the input is affected then the operation would be controlled either by the front or back gate, improving efficiency and achieving low leakage.

IG mode: To increases the flexibility in circuit design and to reduce the number of transistors the front gate and the back gate are given two independent input voltages, respectively.

LP mode: A low voltage is applied to n-type FinFET and high voltage to p-type FinFET back gates. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay.

Hybrid mode: This mode is a combination of IG and LP modes. Because of this, it has the convenient properties of both the modes.

MATERIALS AND METHODS

6T full adder circuit: Numerous full adder circuit designs have been reported using reduced number of transistors as mentioned earlier. A full adder circuit with 6 transistors is presented which uses complementary inputs, hence, requiring additional transistors to invert the input signals. Ultimately a novel 6T design is described in which requires non-complimentary inputs. Their design utilizes the new 2T XNOR gate proposed in that same paper. The 2T XNOR gate and 6T full adder circuits are shown in Fig. 2.

For the 2T XNOR circuit when the PMOS M2 is turned on, it passes the V_{DD} signal and when NMOS M1 is on, it passes the voltage level of input B to the output. For input logics <AB> = <00>, <01> and <11> the output is simply originated from either V_{DD} or input B. However, in the case of <10> combination, both M1 and M2 are on and the output contradicts between 0 from B and 1 from V_{DD}. Because of this improper output logic, M1 is made as strong NMOS by increasing its width higher than that of PMOS.

The 6T full adder circuit, as shown in Fig. 2b, contains 3 modules: two 2T XNOR gates and a 2T MUX. Transistors M5 and M6 together form the MUX. The XNOR output from the first XNOR gate to the gate terminals of M5 and M6 acts as the selection pin. The 2T MUX uses the GDI logic with three inputs and one output. The sum of the full adder is obtained from the 2 cascaded XNOR gates of the three inputs A, B and C. The carry is generated from the 2T MUX. The sum and carry outputs are obtained in accordance to the following equations:

$$\text{Sum} = A \odot B \odot C \quad (1)$$

$$\text{Carry} = A\,(A \odot B) + C\overline{(A \odot B)} \quad (2)$$

It is understood from the design equation that the XNOR and XOR of A, B and C are equal.

RESULTS AND DISCUSSION

The simulation of the 6T FA was carried out using LT spice in PTM 32 nm technology. Circuit parameters and results of the two simulations are discussed in this section.

Simulation using low power MOSFETs: the design was first simulated using PTM-LP MOSFET Model. The widths of the NMOS transistors were taken as 70 µm. The width of PMOS transistor M2 was 0.4 um and widths of PMOS transistors M4 and M6 were 0.04 um. In order to obtain acceptable and desired output logic levels with the above mentioned transistor size parameters, resistors were introduced to the circuit, as shown in Fig. 3, with R1 = 50 k, R2 = R3 = 30 k. The resistors help to pull-down the logic from high to low when input changes from <00> to <01>. If the inputs are interchanged, then the output rises to approximately 300 mV at <10> inputs. In both cases, the resistor is required to maintain the desired logic low at corresponding input combinations. The supply voltage V_{DD} was 1V and the highest input frequency was 1 kHz (input C). The input and output signals are shown in Fig. 4. The final sum and carry outputs obtained from such configurations contained spikes and glitches during logic transitions, as shown in Fig. 5a. In order to eliminate these glitches, capacitors of 0.1 nF were inserted at the final output terminals and the effect is shown in Fig. 5b.

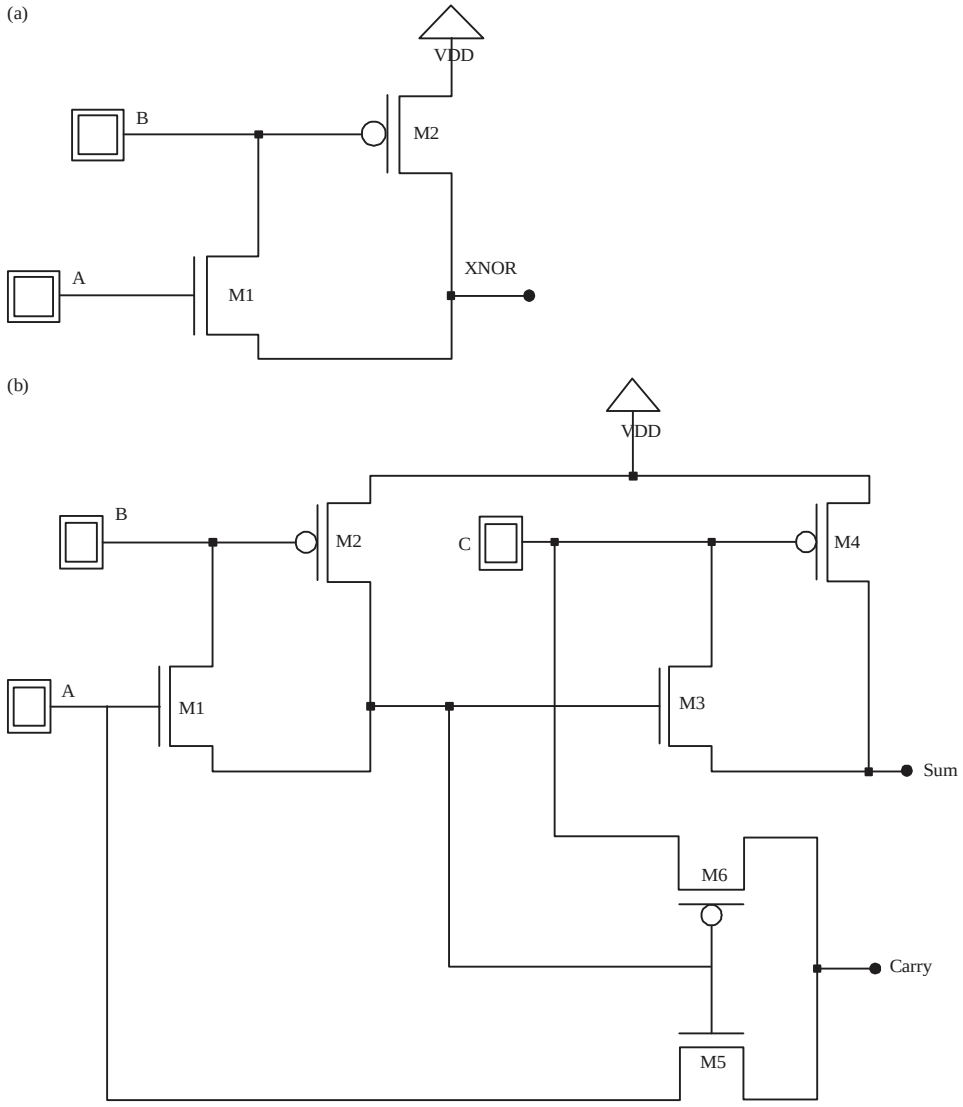

Fig. 2(a-b): (a) 2T XNOR circuit and (b) 6T full adder circuit

It can be observed that the overall output voltage for logic high is very low, approximately 272 mV. Other circuit parameter configurations resulted in a higher but more than one, voltage level for logic high and with big differences in between. The total propagation delay was measured between the time when the changing input reaches 50% of voltage level to the time its output reaches 50% of voltage level for both rising and fall transition for sum and carry. The maximum delay observed for both sum and carry was 2 μsec. The average power consumption of the circuit is 60 μW.

Simulation using DG-FinFETs: After observing the performance with MOSFETs, the 6T FA was next simulated using PTM 32 nm Double-Gate (DG) FinFETs. The MOSFETs in the circuits were replaced by a sub-circuit model representing the DG FinFETs. Transistor sizes were manipulated from the previous chosen ones for good, desired output. The width of NMOS transistors M1, M3 and M5 were taken 5 μm, more than 10 times less than previous. The width of PMOS transistors M2, M4 and M6 were taken 0.4, 0.12 and 0.06 μm, respectively. All other circuit variables remained same as before.

As mentioned earlier, FinFETs have different modes of operation: SG, LP, IG and hybrid mode. The SG mode was first used to simulate and the output is shown in Fig. 6. The output voltage level is good at more than 70% of V_{DD}. This indicates the advantage of FinFETs giving a voltage gain. As a consequence, the zero logic voltage level rises slightly above 0 V. However, the merits of using FinFETs come at the cost of high average power consumption of 144.3 μW.

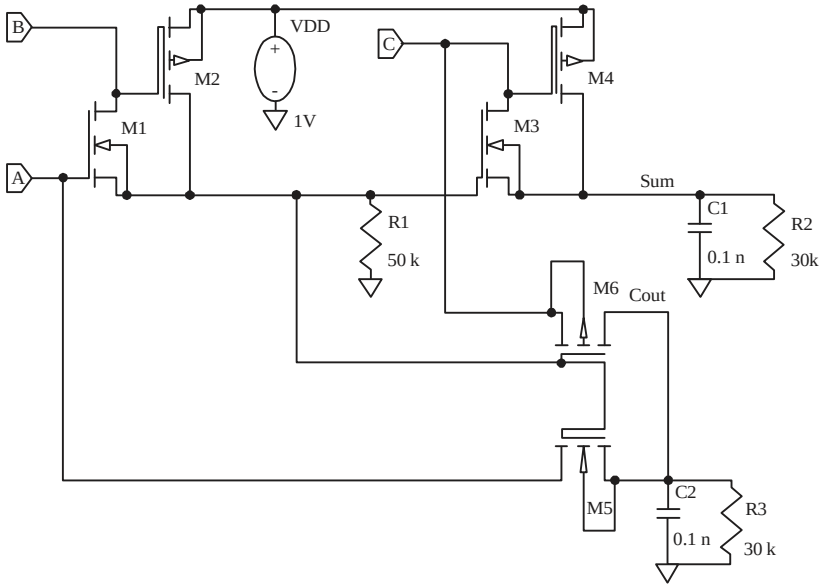

Fig. 3: 6T full adder simulation circuit with PTM-LP 32 nm MOSFETs

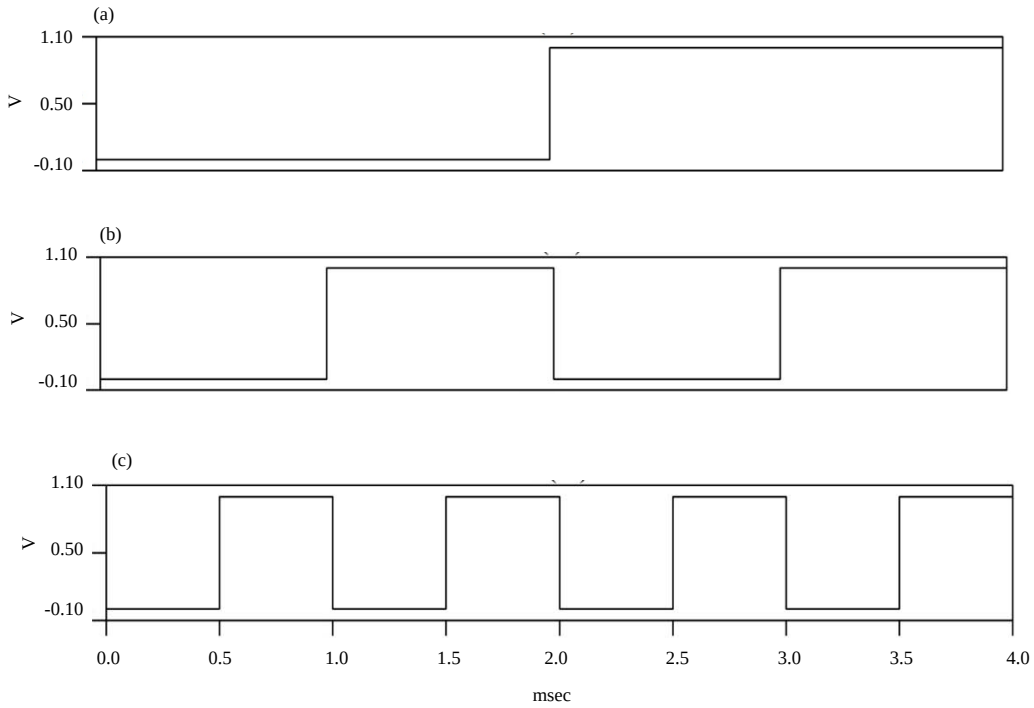

Fig. 4(a-c): Input signals (a) Va, (b) Vb and (c) Vc

Next, the LP mode of operation of FinFETs was observed in the circuit. The back gates of n-type transistors were grounded and the back gates of p-type transistors were applied a positive 1 V. As a result the power consumption reduced significantly to 27.5 uW but the output voltage for logic 'high' varied for different combinations, as shown in Fig. 7.

Finally, the hybrid mode of operation was simulated. This involved both SG and LP modes. The SG mode was used for the n-type FinFETs and the LP mode was used for the p-type FinFETs. The exact output of SG mode was obtained with slight manipulation in transistor size. The width of transistors M4 and M6 were taken 0.2 µm and 0.12 µm, respectively. The average power consumption was 76.6 µW.

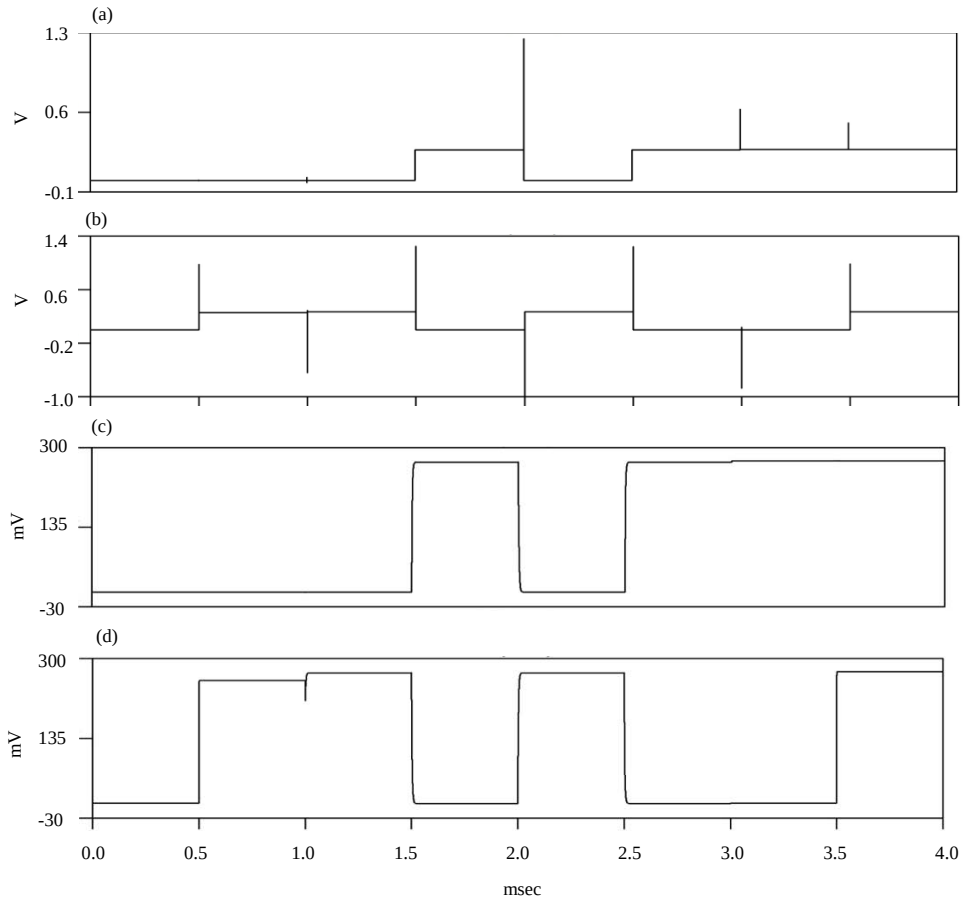

Fig. 5(a-d): V(cout) and V(sum) outputs using PTM-LP 32 nm MOSFETs (a, b) Without capacitors, (c, d) With capacitors

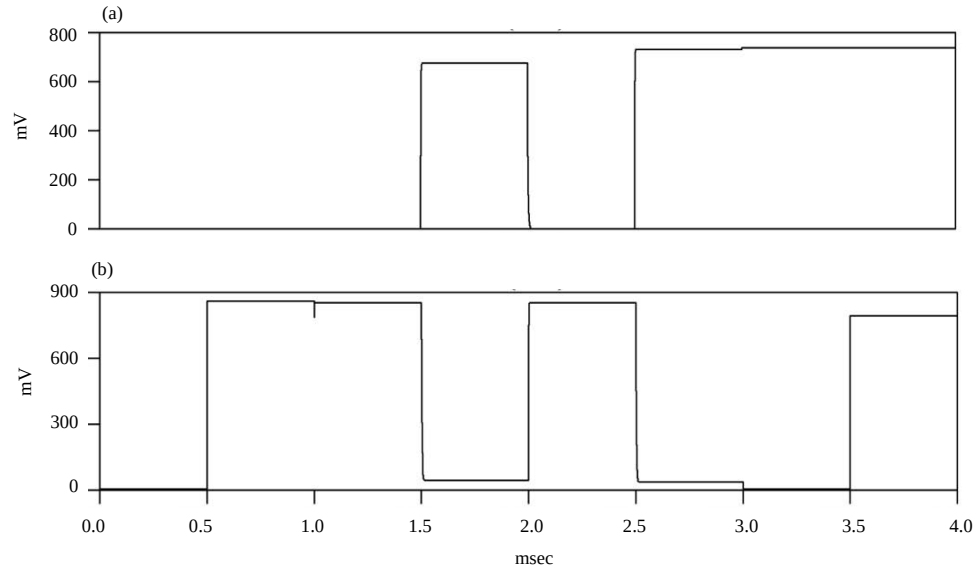

Fig. 6(a, b): Outputs using PTM 32 nm DG FinFET (SG mode) (a) V(cout) and (b) V(sum)

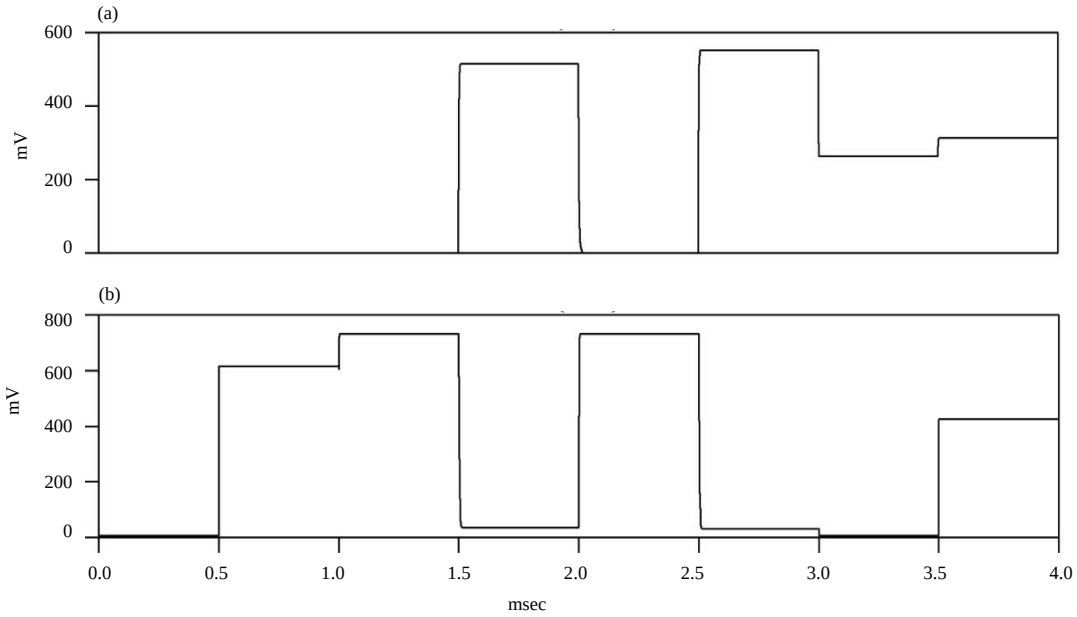

Fig. 7(a, b): Outputs using PTM 32 nm DG FinFET (LP mode) (a) V(cout) and (b) V(sum)

Table 1: Performance comparison between MOSFET and FinFET (Supply voltage = 1 V)

Parameters	MOSFET	FinFET
Power consumption (μW)	60	SG: 144.3
		LP: 27.5
		Hybrid: 76.6
Delay (μsec)	Sum: 2	Sum: 2
	Carry: 2	Carry: 1
Voltage for output logic high (V)	Sum: 0.27	Sum: 0.85
	Carry: 0.27	Carry: 0.73 (SG mode)

Performance comparison: A performance comparison between MOSFET and FinFET is provided in Table 1. The use of PTM-LP MOSFETs in the 6T FA circuit shows promising results in terms of power requirement at the cost of significant output voltage level degradation. On the contrary, the use of FinFETs provide better performance in terms of size, speed (carry output) and output voltage level and uniformity at the cost of high power dissipation. The optimum performance in terms of both power requirement and voltage level is obtained when FinFETs are operated at hybrid mode.

CONCLUSION

The 6T FA design proposed in a previous research delivers as a desirable full adder circuit with performance enhancement in terms of power consumption, speed and area. However, performance analysis shows that the circuit requires extra passive elements and proper manipulation of transistor sizes in order to achieve the desired output logic. Comparative analysis between MOSFETs and FinFETs shows that much smaller size FinFETs, more than 10 times less than MOSFET transistors, give expected output with better output voltage at similar speed. Hence, the overall area of the circuit with FinFETs can be reduced at great amount. Although, FinFETs provide good alternatives to the bulk CMOS, the PTM-LP MOSFETs deliver better power consumption than the PTM DG-FinFETs being successful in their designed purpose. The performed simulation gives more stable and uniform output voltage level with the 6T design than in previous research.

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