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Fuzzy-PI Based DVR Setup for Voltage Dip and Voltage Swell Problems with Hardware Comparison

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Abstract: Power quality issues have been pulling in the eye of investigates for decade. The nearness of voltage unsettling influences at the purpose of normal coupling brings about glitch of delicate modern instruments which ends up being matrix part disappointments. Although, there are many strategies in practice, the term custom power relates to the utilization of energy hardware controller in an appropriate framework, particularly to manage different power quality issues. Now the custom power devices play a vital role in the field of power quality mitigation. The presence of sensitive loads lead to the power quality issues like sag and swell but it is inevitable. DVR is one of the popular and efficient custom power devices most suitable distribution network to mitigate the voltage dip and swell. Fuzzy based PI control is incorporated in this study. The main salient feature is the use of linguistic variables rather than numerical variables. This control method depends on human capacity to comprehend the frameworks conduct and depends on quality control rules. An experimental investigation on the mitigation of sag and swell by using three phase Dynamic Voltage Restorer (DVR) is proposed in this study. It is observed that the compensating capability of the DVR is somewhat lagged due the finite voltage dip under particular loading. A fuzzy based PI scheme is therefore proposed to improve the voltage compensation. The simulation result is appraised with experimental results and it presented it witnessed the effectiveness of the control strategy.

Key words: Power Quality PQ, Point of Common Coupling (PCC), Dynamic Voltage Restorer (DVR), fuzzy logic controller Fuzzy Logic (FL), mitigation, Dynamic Voltage Restorer (DVR)

INTRODUCTION

Power quality issues are an issue that is winding up progressively vital to power customers at all levels of use. Power quality issues have been pulling in the eye of looks into for decade. Power quality related issues are of most trouble in view of the broad utilization of electronic equipment. The various power quality disturbances which affect the quality of power are listed as voltage drop, voltage swell, voltage flickering long and short duration interruptions, presence of harmonics and unbalanced voltages. In the researcher investigates the design requirement of the DVR scheme for mitigating the power quality issues in power distribution system. The researcher perfomed many case study on the basis of the DVR topology and control schemes (Li *et al*., 2007) studied the transient responses of the DVR based on this study control schemes are proposed to alleviate the voltage dip and suppress the high frequency oscillation. Mangalanathan (2014) proposed a MOSFET based single phase DVR design for the mitigation of voltage sag and swell. The MOSFET was triggered by the microcontroller based PWM technique. The power quality issues are generated by creating the fault in the system. Roncero-Sanchez *et al*. (2009), A repetitive controller based on the control system scheme is suggested for Dynamic Voltage Restorer (DVR) to compensate the harmonics, sags in voltage and imbalance voltages. In the researcher addressed the restoration capability of the DVR during the power quality issue occurred in the distribution system. Devadasu and Sushama, (2015) suggested a three phase DVR topology energized by multilevel inverter with five level output. Here, the researcher used the power compensation at minimum level in order to reduce the energy storage requirement of the multilevel DVR. Mostafa *et al*. proposed a new DVR topology based on H-bridge cascaded multi level inverter. Here, the DVR topology is enhanced by the absence of transformer with energy optimized control scheme. This scheme reduces the ride through capability of the DVR.

Devadasu and Sushama, (2017a-d) Diode clamped multilevel converter IDVR is suggested for the power quality problems like sag swell. In this scheme the load power factor is reduced during sag o swell condition in turn increases the compensation capacity. Moreover, in

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this research SVPWM technique is employed in the IDVR scheme to inject the voltage with low THD which avoids the presence of isolation transformer in one side. This study discusses the power quality issues created when the renewable resources integrated with the distribution system. The research also analyzes the different mitigation methodology with custom power devices. In Lachlan *et al.* discussed the technique of identifying power quality disturbances in terms of time and frequency using the wavelet based on the software analysis. Omar *et al.* discussed the role of DVR in the low voltage distribution system during power quality disturbances. Here, the DVR employs an advance dq0 control strategy. The simulation result is appraised with the hardware result of the DVR set up. Devadasu and Sushama, (2018), the emphasized the DVR with fuzzy logic control strategy. Fuzzy logic provides an easy way to reach the desire conclusion even though the input is vague and ambiguous (Devadasu and Sushama, 2015; Devadasu and Sushama, 2017a-d).

MATERIALS AND METHODS

Mitigation of power quality problems: DVR is a static series compensator which is used to remove supply side voltage disturbances and also keeps the load side voltage at a desired magnitude and phase by compensating the voltage sags/swells at PCC (Fig. 1).

Injection/Booster transformer: The injection/booster transformer is used to transfer the energy from primary side to secondary and to reduce the coupling noise. This unit makes the connection between DVR and distribution network through the high voltage winding and injects the compensating voltage generated from the VSC to the supply side.

Harmonic filter: It is used to keep the harmonic voltage generated by the VSC within the admissible level. When large voltage source occurs the storage devices-such as flywheels, batteries will provide the real power compensation.

Voltage source converter: It consists of storage and switching devices. It is used to provide a sinusoidal voltage at any needed magnitude, frequency and phase angle. Here, VSC provide the temporary compensation or part of the voltage which is needed for the compensation.

DC charging circuit: It plays two vital role of charging the energy source after the compensation and maintains the DC link voltage at nominal level.

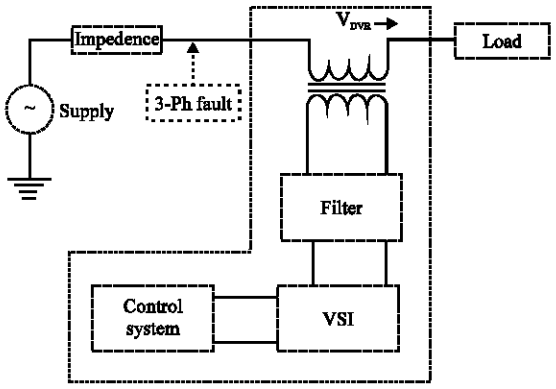

Fig. 1: Schematic diagram of a dynamic voltage restorer

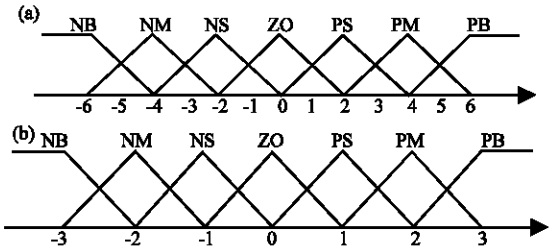

Fig. 2: Membership functions of the fuzzy variable: a) Membership function of ΔK_p and ΔK_i and b) Membership function of e(K) and $e_c(K)$

Control and protection: It provides all necessary protection to the DVR by the hardware and programe logic software.

Control scheme of DVR: The control scheme is designed in such a ways to ensure the balance, constant linear nature of the load voltage and current. Also, ensure the zero phase difference between source current and fundamental component of PCC voltage. To do so, the reactive power of the load is met by the DVR.

From the real system the error 'e' and change of error 'ec' are used as numerical variables. The conversion of numerical variables in to linguistic variables is done by adopting the following fuzzy sets: Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (ZE), and Positive Small (PS), Positive Medium (PM) and Positive Big (PB). The membership function of the fuzzy sets is chosen in such a way to confirm the robustness and sensitivity of the controller. e(K), $e_c(K)$, ΔK_p and ΔK_i in this study are acquired from the ranges of e, e_c, ΔK_p and ΔK_i which are obtained from study and experience. And the membership functions are shown in Fig. 2. The important factors considered for designing the control rule base for tuning ΔK_p and Δk_i:

- A small change in K_p is enough for small values of error |e| at the same time for large values of error |e| a large ΔK_p is required
- If $e\text{-}e_c>0$, then ΔK_p is large and If $e\text{-}e_c<0$ then ΔK_p is small
- if |e|and $|e_c|$ are large then ΔK_I is zero
- ΔK_I is effective when the values of |e| is small and ΔK_I is larger when |e| is smaller which is better to decrease the steady-state error. So, the tuning rules of ΔK_p and ΔK_I can be shown below in Table 1 and 2.

Constant band width hysteresis control method has high switching frequency which leads to the system loss. For that here the fuzzy controller is used. This controller also I improve the behavior of DVR and also produce the five level converters output. The one input of the fuzzy controller is difference of injected and reference voltage another input is derivative of error.

Table 1: The rule for adjusting ΔK_p

	e_c						
Δkp (e)	NB	NM	NS	0	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	0
NM	PB	PB	PM	PM	PS	0	NS
NS	PM	PM	PS	PS	0	NS	NM
0	PM	PS	PS	0	NS	NM	NM
PS	PS	PS	0	NS	NS	NM	NM
PM	PS	0	NS	NM	NM	NM	NB
PB	0	NS	NS	NM	NM	NB	NB

Table 2: The rule for adjusting ΔK_I

	e_c						
ΔK_I (e)	NB	NM	NS	0	PS	PM	PB
NB	0	0	NB	NM	NM	0	0
NM	0	0	NM	NM	NS	0	0
NS	0	0	NS	NS	0	0	0
0	0	0	NS	0	PS	0	0
PS	0	0	0	PS	PS	0	0
PM	0	0	PS	PM	PM	0	0
PB	0	0	PS	PM	PB	0	0

The controller directly turns on or turns off the switches based on the voltage condition by considering the difference between converter output voltage and reference voltage and its derivation. In conventional hysteresis voltage control method, switching signals are generated when the error reaches to upper or lower hysteresis band but as shown in Fig. 3 in this proposed method generate the switching signals based on the value of the error and derivation of the error.

The main considerations for the control system of a DVR include detection of sag/swell, voltage reference generation, transient and steady-state control of the injected voltage and protection of the system.

Simulation circuit: Usually, due to switching on and switching off of loads and nonlinear loads power quality problems are occurring. Increase in load creates a sag whereas sudden removal of load creates a swell. At once the sag or swell is occurred at load side, the magnitude of the voltage is compared with the reference signal. The error between these two is given as an input to the PI controller. The PI controller voltage is taken as feedback. The PI controller based on fuzzy is the most frequently used controller in the DVRs. The performance of PI controller under wide range of operating condition is not appreciable. This drawback is overcome by the proposed fuzzy-PI controller. In this control method, PLL tracks the phase angle of all three phases of the network and based on that it generates the reference signal for each phase.

It is because, the phase of the supply voltage prior to the sag is usually chosen and if the PLL reacts swiftly to changes in the phase during sag, the post-sag phase may

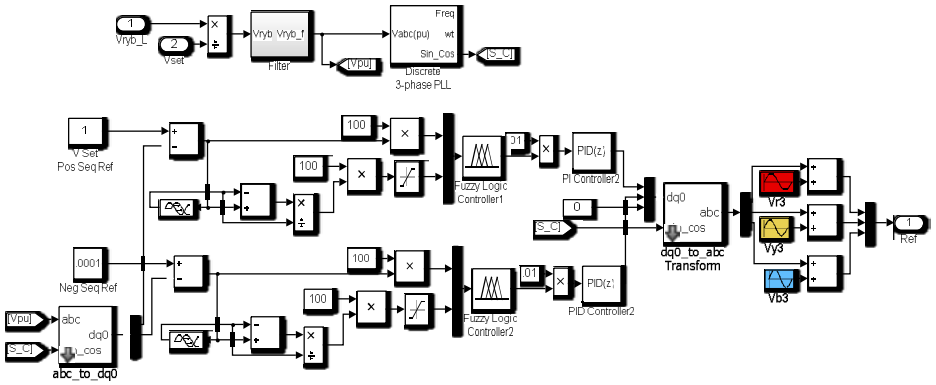

Fig. 3: Control structure of DVR

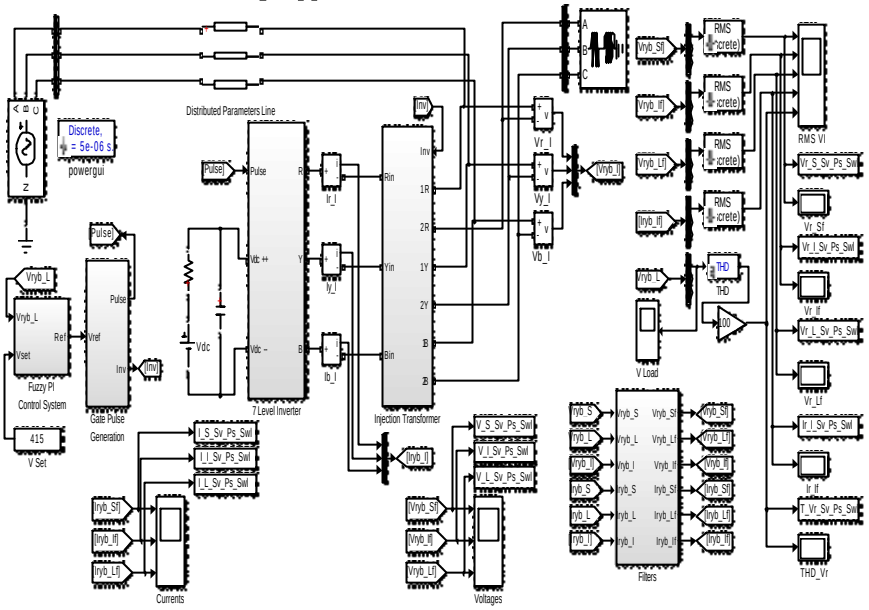

Fig. 4: Simulation diagram-dynamic voltage restorer

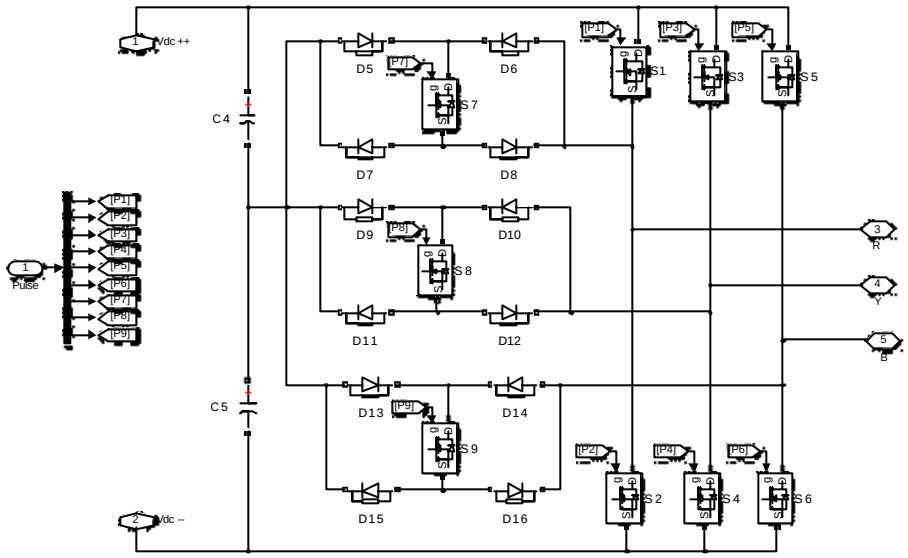

Fig. 5: Seven-level converter based DVR system

be used. Normally, once sag is detected, the target phase of the voltage reference is fixed to the pre-sag phase to ensure that if the reference is tracked correctly then the load voltage phase will remain unaltered. In this study, the control strategy applies the pre-sag compensation to maintain the pre fault value. The simulation diagrams of voltage sag and swell in closed loop system is as shown Fig. 4.

Dynamic Voltage Restorer (DVR): Is one of the most efficient and effective contemporary custom power devices used in power distribution networks. This study mainly discusses about the Power Quality (PQ) problems mitigation algorithm (Fig. 5 and Table 3).

Table 3: Switching states for seven level inverter

	Switches								
Time slot	S1	S2	S3	S4	S5	S6	S7	S8	S9
T1	1	0	0	1	1	0	1	1	0
T2	1	0	0	1	1	0	0	1	1
T3	1	0	0	1	0	1	1	0	1
T4	1	0	0	1	0	1	1	1	0
T5	1	0	1	0	0	1	0	1	1
T6	1	0	1	0	0	1	1	0	1
T7	0	1	1	0	0	1	1	1	0
T8	0	1	1	0	0	1	0	1	1
T9	0	1	1	0	1	0	1	0	1
T10	0	1	1	0	1	0	1	1	0
T11	0	1	0	1	1	0	0	1	1
T12	0	1	0	1	1	0	1	0	1

Source side power quality problems can be regulated when these voltages are injected in series with a distribution feeder by a Voltage Source Inverter (VSI) with SPWM, control, third order injected SPWM and third order injected phase shift SPWM and there by regulating the voltage at the load terminals. This technique analyse the power circuit, possible control limitations and control targets before providing the compensating control through DVR. The multilevel inverter is chosen for their following merits like less distorted output, low dv/dt, low distorted input current and smaller common mode voltage.

RESULTS AND DISCUSSION

The control scheme of the DVR is implemented through derived reference load terminal voltages. The multi-level scheme is a trouble-free design. Simulation results carried out by MATLAB with its Simulink and Sim Power System (SPS) tool boxes to verify the performance of the multi-level method.

Case 1: Mitigation of power quality problems by DVR with SPWM.

Case 2: Mitigation of power quality problems by DVR with third order injected SPWM.

Case 3: Mitigation of power quality problems by DVR with third order injected phase shift SPWM. From the above figures i.e., Fig 6-29 it is observed that, first, waveform is the voltage sag/swell is introduced at 0.1 sec and continued up to 0.4 sec for the time period of 0.3 sec. Second, waveform is the voltage induced is produced at 0.1 sec and continued up to 0.4 sec for the time period of 0.3 sec, third, wave form is the voltage level of load voltage from the time period 0.025-0.5 sec is maintained required level.

Experimental power circuit 3 phase DVR: The following are the main components used the experimental power circuit 3 phase DVR:

- Signal conditioning circuit
- Source transformers
- ARM micro controller
- DC link
- Series inverter
- Injection transformers
- Source transformers
- Pulse driver
- Line feeders
- Resistive load

As shown in Fig. 30, the hardware block diagram mainly consists of LPC2148-ARM (Advanced RISC machine) controller as CPU (Central Processing Unit) equipped with 2-line and LCD control keys. Potential transformers are used to apprehend the source and load voltages. They are further given to internal analog to digital converter of ARM controller and after signal conditioning. To apprehend the zero crossing of AC voltage and also to progress an interrupt signal to ARM controller a zero crossing detector is used. The main objective of ZCD is to adjust the generated wave of inverter for every start of each source cycle. By acquiring the signal of interrupt the output of the inverter will be adjusted with positive source cycle for sag condition and negative source cycle for swell condition. Zero crossing detectors are provided at each single phase. To choose the required or necessary sag and swell mode of operation various control keys are used. Apart from selection they are also used set the required voltage in the system. LCD displays the ideal and practical voltages and the required message during operation. For practical analysis, a 3-phase star connected source of rating 230 V/48 V, 3A per phase and 1 oad as 3-phase star connected resistive with rating 48 Ω, 48 W per phase is selected as AC source

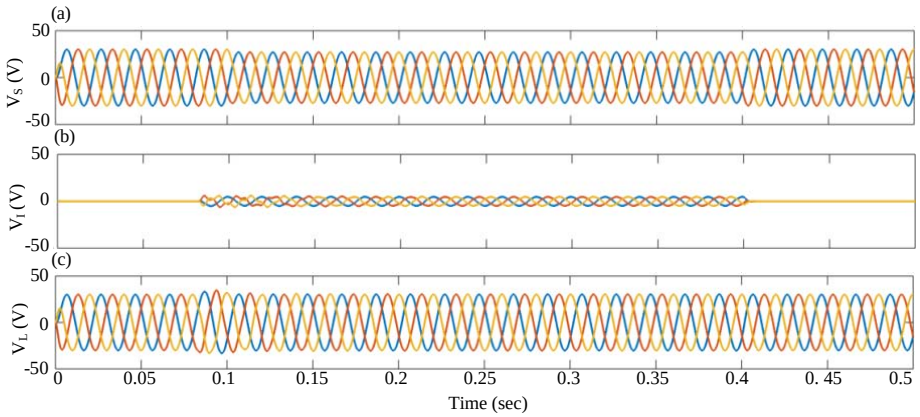

Fig. 6: a-c) Imulation results-DVR with SPWM for sag (10%) voltage

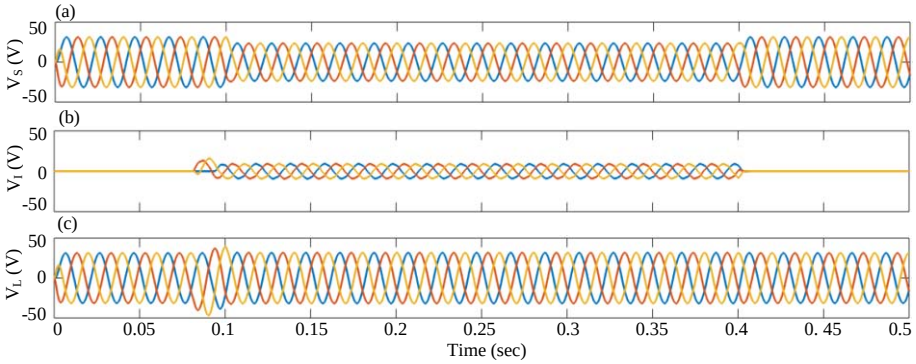

Fig. 7: a-c) Simulation results-DVR with SPWM for sag (25%) voltage

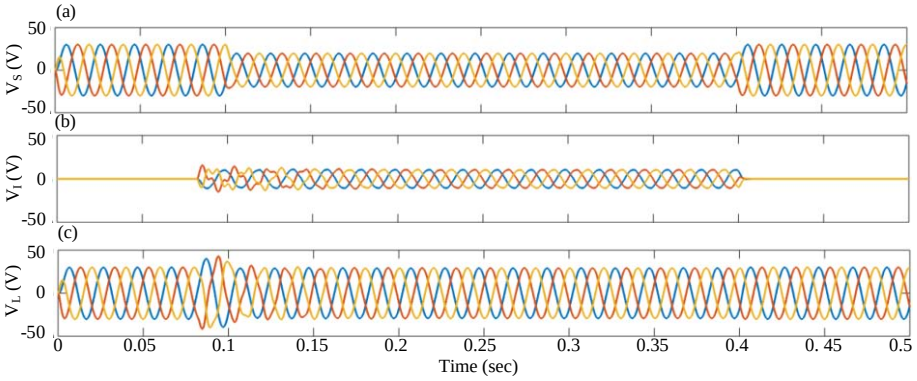

Fig. 8: a-c) Simulation results-DVR with SPWM for sag (35%) voltage

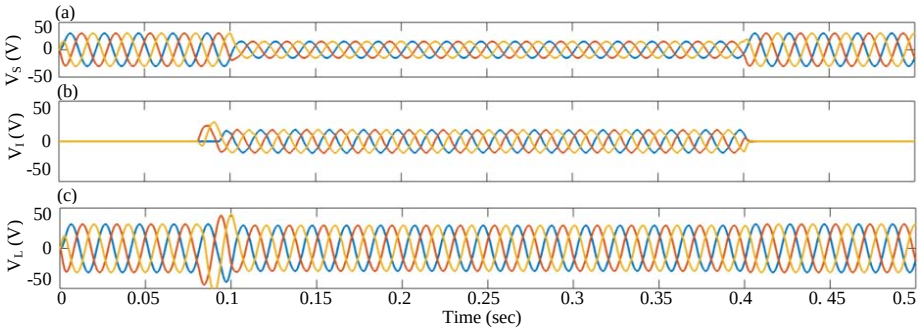

Fig. 9: a-c) Simulation results-DVR with SPWM for sag (50%) voltage

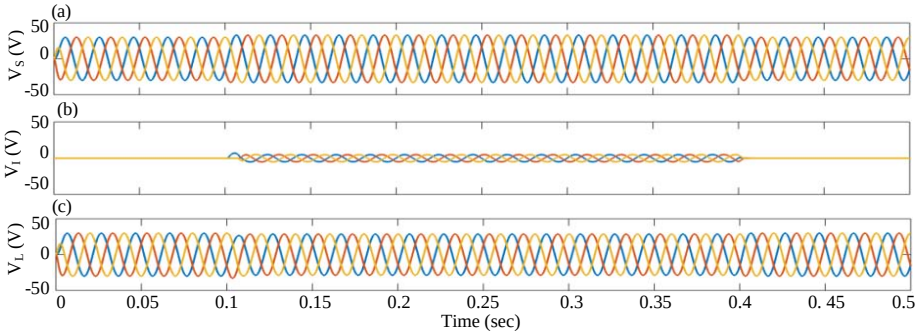

Fig. 10: a-c) Simulation results-DVR with SPWM for swell (10%) voltage

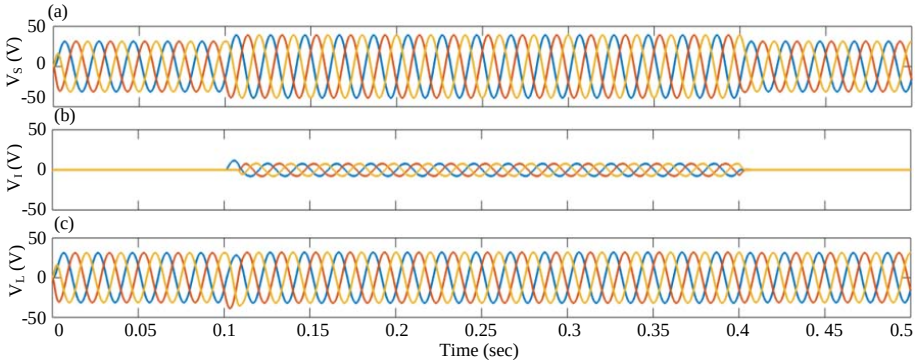

Fig. 11: a-c) Simulation results-DVR with SPWM for swell (25%) voltage

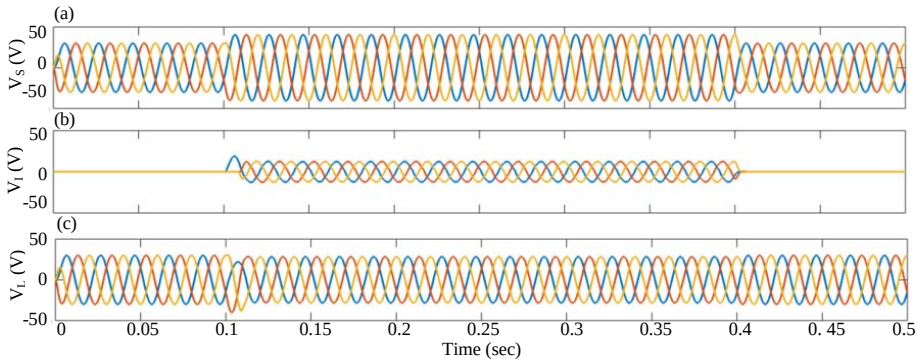

Fig. 12: a-c) Simulation results-DVR with SPWM for swell (35%) voltage

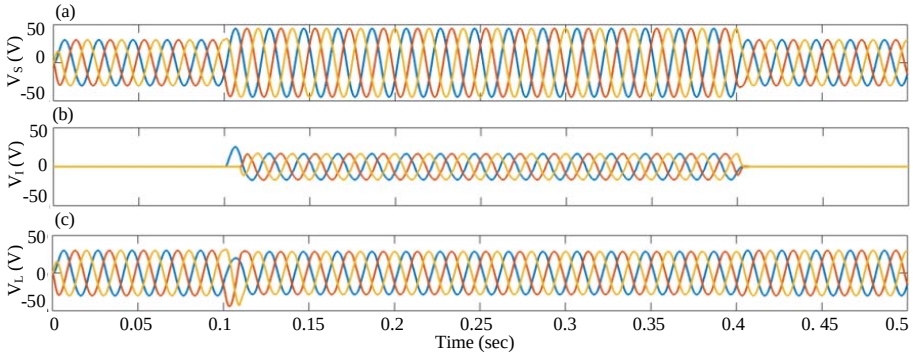

Fig. 13: a-c) Simulation results-DVR with SPWM for swell (50%) voltage

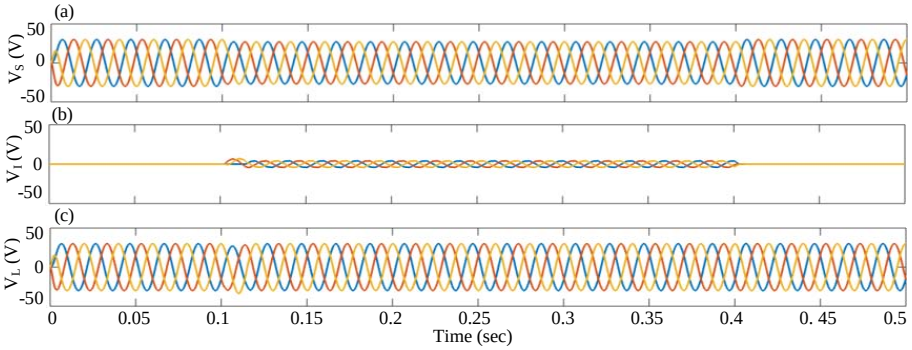

Fig. 14: a-c) Simulation results-DVR with third order harmonics injected SPWM for sag (10%) voltage

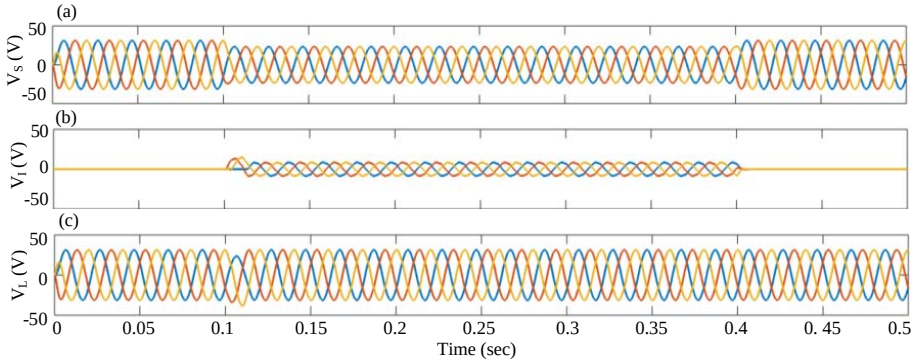

Fig. 15: a-c) Simulation results-DVR with third order harmonics injected SPWM for sag (25%) voltage

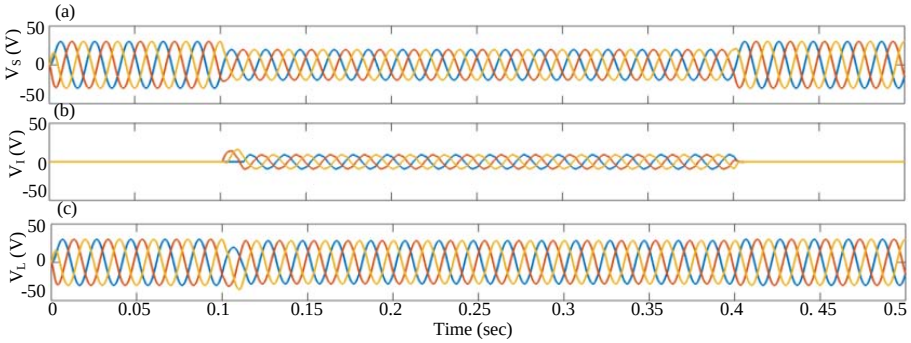

Fig. 16: a-c) Simulation results-DVR with third order harmonics injected SPWM for sag (35%) voltage

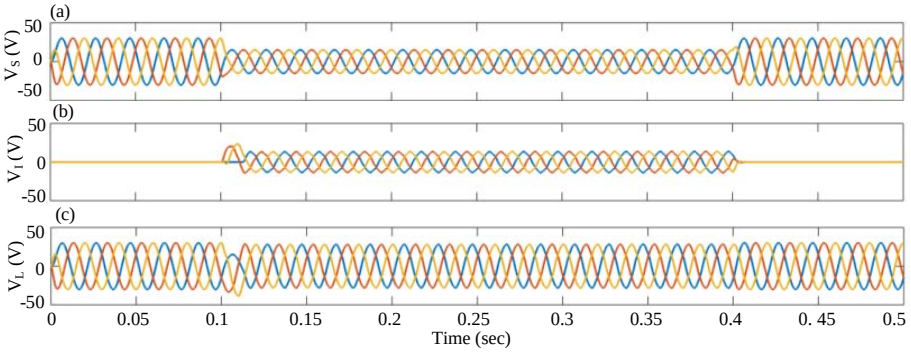

Fig. 17: a-c) Simulation results-DVR with third order harmonics injected SPWM for sag (50%) voltage

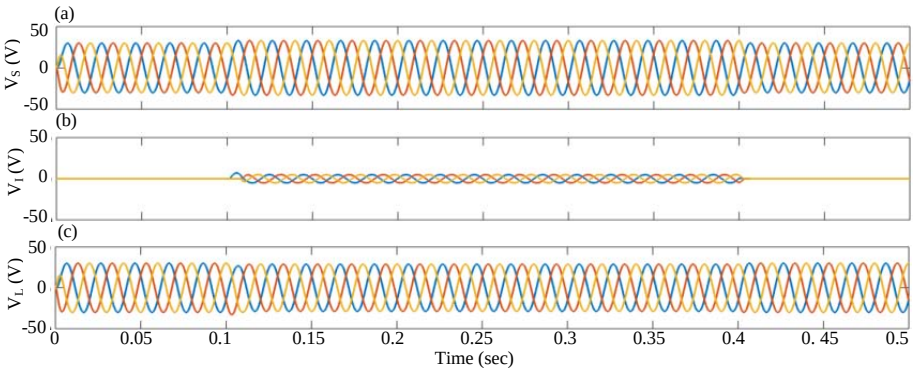

Fig. 18: a-c) Simulation results-DVR with third order harmonics injected SPWM for swell (10%) voltage

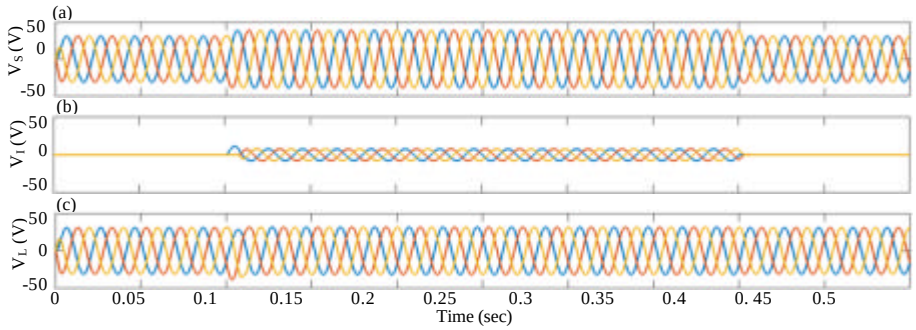

Fig. 19: a-c) Simulation results-DVR with third order harmonics injected SPWM for swell (25%) voltage

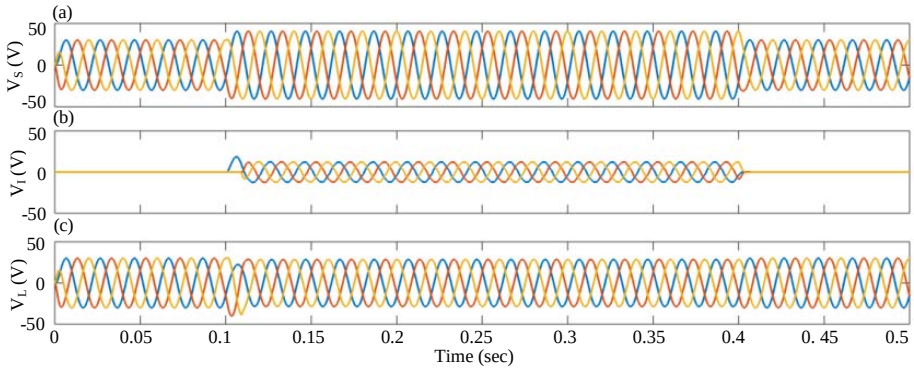

Fig. 20: a-c) Simulation results-DVR with third order harmonics injected SPWM for swell (35%) voltage

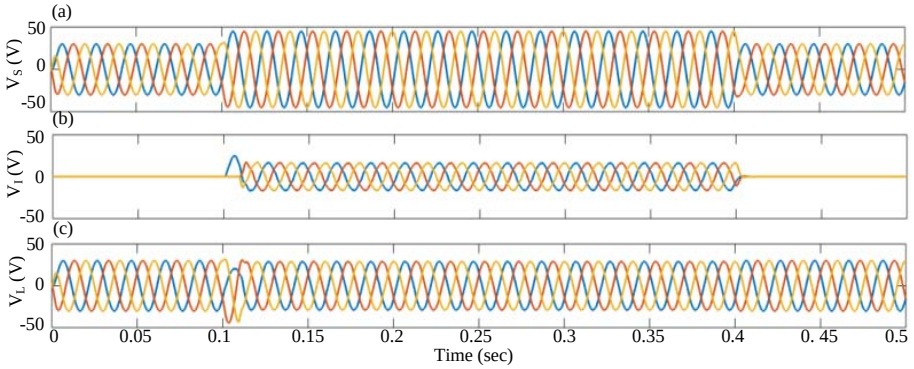

Fig. 21: a-c) Simulation results-DVR with third order harmonics injected SPWM for swell (50%) voltage

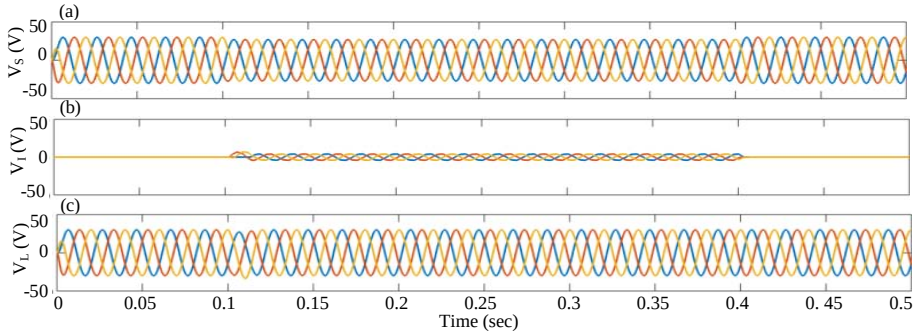

Fig. 22: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for sag (10%) voltage

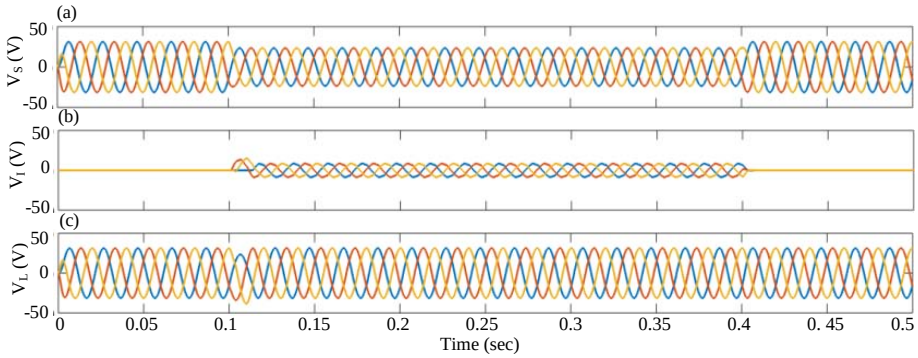

Fig. 23: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for sag (25%) voltage

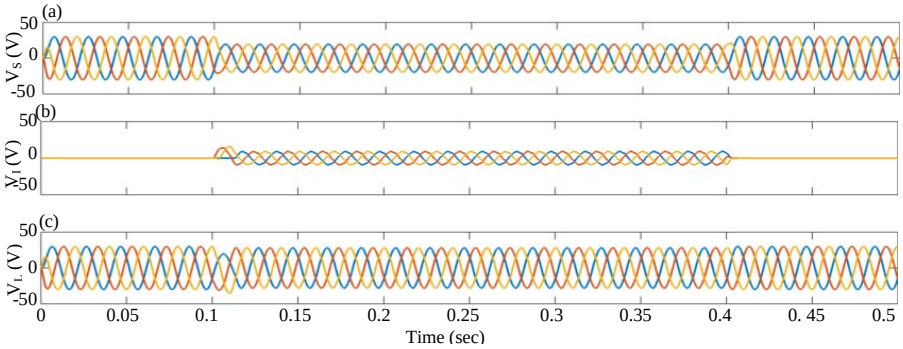

Fig. 24: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for sag (35%) voltage

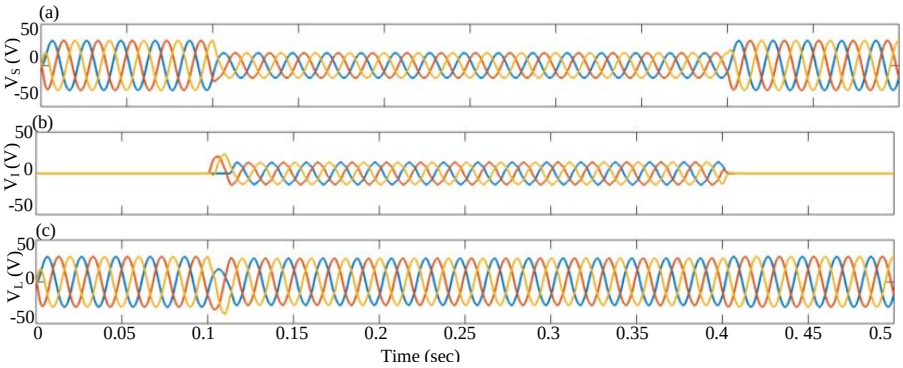

Fig. 25: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for sag (50%) voltage

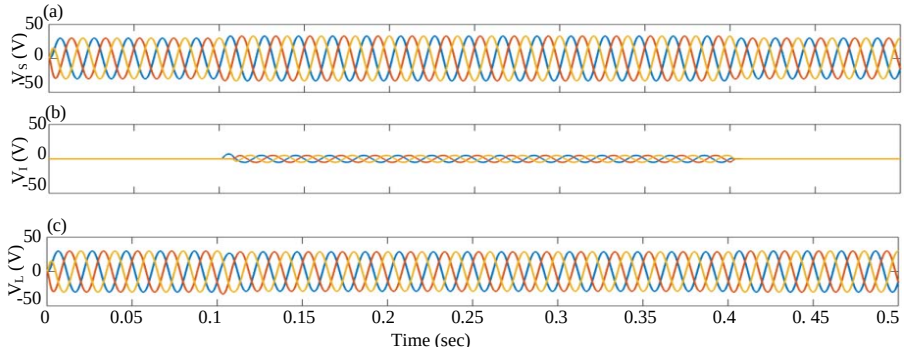

Fig. 26: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for swell (10%) voltage

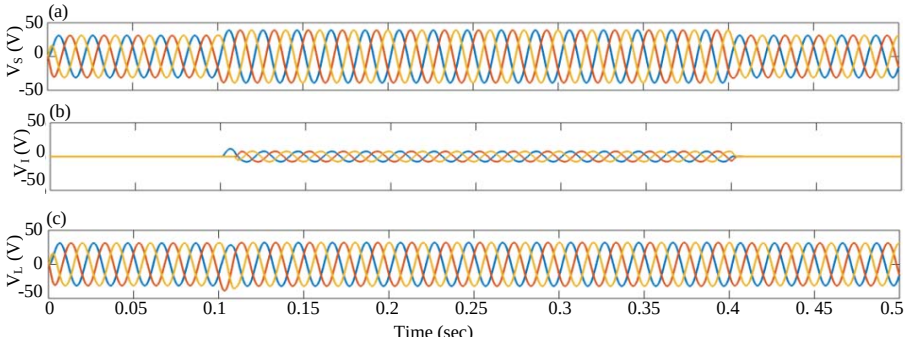

Fig. 27: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for swell (25%) voltage

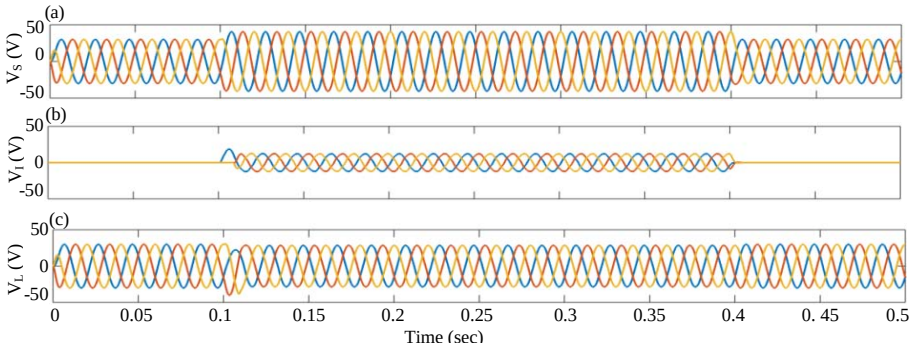

Fig. 28: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for swell (35%) voltage

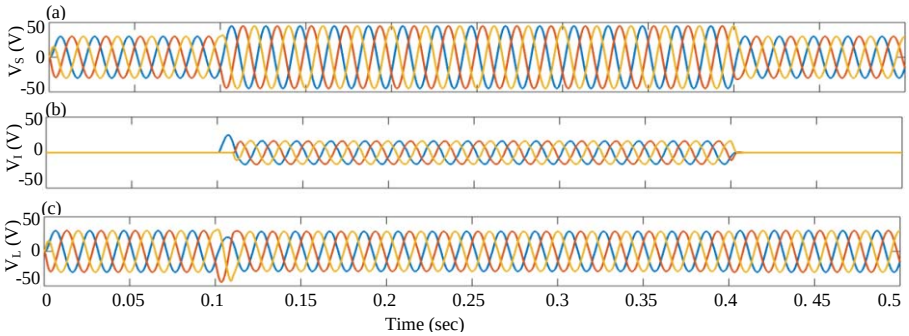

Fig. 29: a-c) Simulation results-DVR with third order harmonics injected phase shift SPWM for swell (50%) voltage

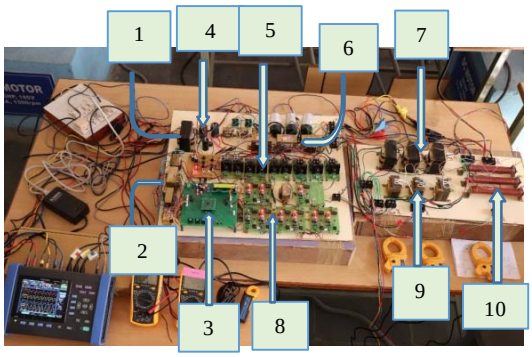

Fig. 30: Experimental 3 phase power circuit DVR

load. Injection transformer of rating 48 V/48 V, 3 A per phase is selected. In this experimental analysis a 7-level inverter is designed by coupling the three bidirectional switches to traditional 6-pulse 3-phase bridge inverter with 6-unidirectional switches. The topography of the designed inverter is shown in Table 4. In the designed inverter, the switches S1-6 are the MOSFET IRF460P unidirectional switches with suitable snubber circuit.

Whereas the switches S7-9 are bidirectional switches in which one MOSFET IRF460P power switch and four high frequency switching power diodes UF5408 are used. The traditional 6-pulse inverter produces 5-level phase voltage and the arrangement of bidirectional switch to each phase produces an extra level in positive and

negative cycle. Hence, it results in increase in number of voltage levels in phase voltage to seven and therefore, minimizes the content of harmonics. Two series Capacitors C1 and C2 with identical rating are connected across the inverter DC source to produce the necessary voltages required for bidirectional switches.

ARM controller produces gate pulses of a voltage level 3.3 V. But the MOSFETs desires a gate pulse of magnitude 10-20 V. Hence, to overcome this problem, a gate driver circuit with OPTO coupler is designed to increase the level of gate pulse suitable for MOSFETs and also for isolation of ground. Each and every power switch consists of individual driver circuit with an isolated power supply. Fuzzy-PID controller is used to control the gate switching pulses produced by the ARM controller. In this setup, the timing pulses produced by the internal timer of ARM controller for the time duration of 20 msec (1/50 Hz = 20 msec) is further splitted into 12 time slots (6 time slots for positive cycle and 6 for negative cycle). These timing pulses symbolize SVPWM phase angles. By using the PWM unit of ARM controller, 10 kHz modulating triangular pulse width modulation signal is produced. The generated timing pulses can be amplified or modulated externally using OR gates (Fig. 31-49 and Table 5 and 6).

Table 4: Three phase dvr components

Name of the equipment	Range	Qty
Power Transformer (PT)	230 V/24 V-0-24 V, 3A	1
Inductance (Line impedance)	4 mH	3
Resistive load	96 Ω	3
DC link capacitors		
Filter capacitor	2220 µF, 100 V	1
Capacitance	10000 µF, 50 V	2
Series inverter		
Unidirectional MOSFET	IRF 460- 460 V, DC, 10 Amps	6
Bidirectional MOSFET	IRF 460-460 V, DC, 10 Amps	3
Firing circuit		
Diode	IN4007	9
Capacitor	470 µF, 25 V	9
Regulator	7805, 5 V, 500 mA	9
Regulator	7812,12 V, 500 mA	9
Filter	100 µF	9
Opto isolator	6N137-8 pin	9
Transistor	2N3904	9
Firing chip component	IC IR2100	9
Signal conditioning circuit		
Step down transformer	230V/12V,_A	1
Operational amplifier	LM358	1
Input voltage measurement		
Isolation transformer	9 V-0-9 V/9 V-0-9 V, 500 mA	1
Power supply for µc–Power transformer	230 V/9 V, 1A.	1
Power supply for firing circuit–Step down transformer	230 V/12 V, 250 mA	2
Power supply for signal conditioning circuit	230 V/12 V-0-12 V, 1A	1
Bridge rectifier	BR1010	1
Micro processor	LPC2148-ARM	1

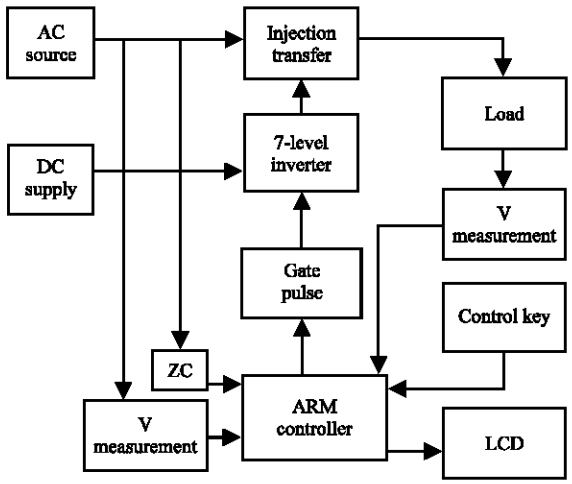

Fig. 31: Hardware block diagram

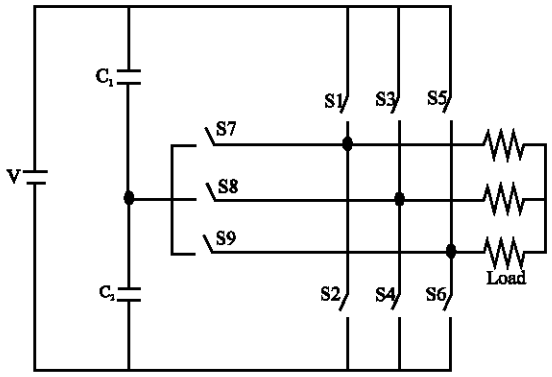

Fig. 32: Topology of 7-level inverter

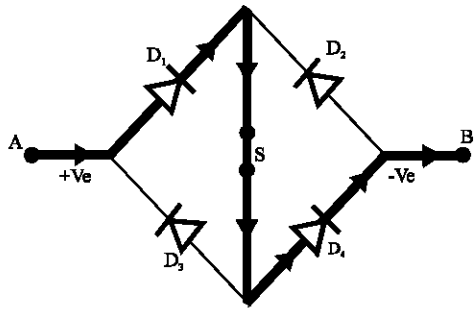

Fig. 33: Conduction a to b

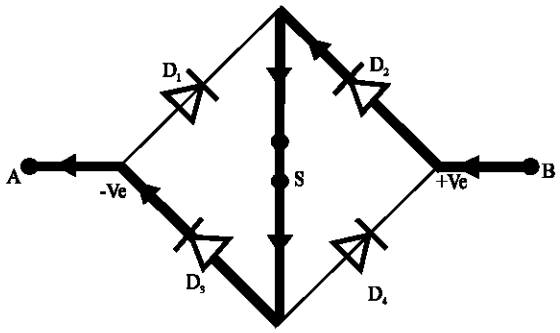

Fig. 34: Conduction b to a

Fig. 35: Experimental results-DVR with SPWM for swell (36%) Total Harmonic Distortion (THD)

Fig. 36: Experimental results-DVR with SPWM for swell (36%) voltage without compensation

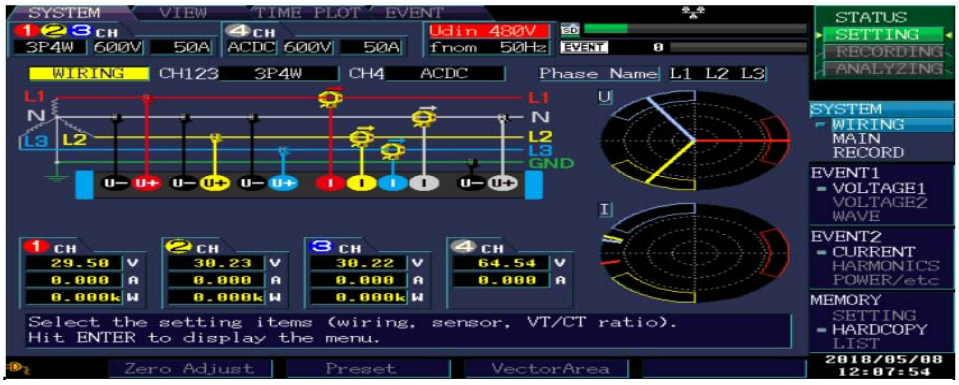

Fig. 37: Experimental results-DVR with SPWM for swell (36%) voltage with compensation

Fig. 38: Experimental results-DVR with SPWM for swell (16%) Total Harmonic Distortion (THD)

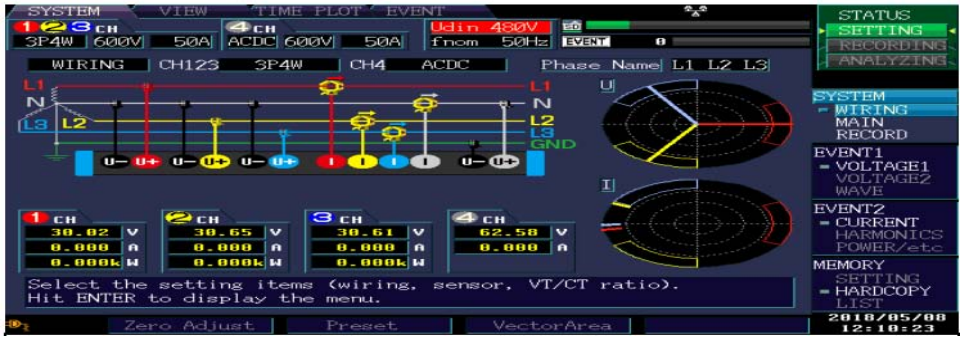

Fig. 39: Experimental results-DVR with SPWM for swell (16%) voltage without compensation

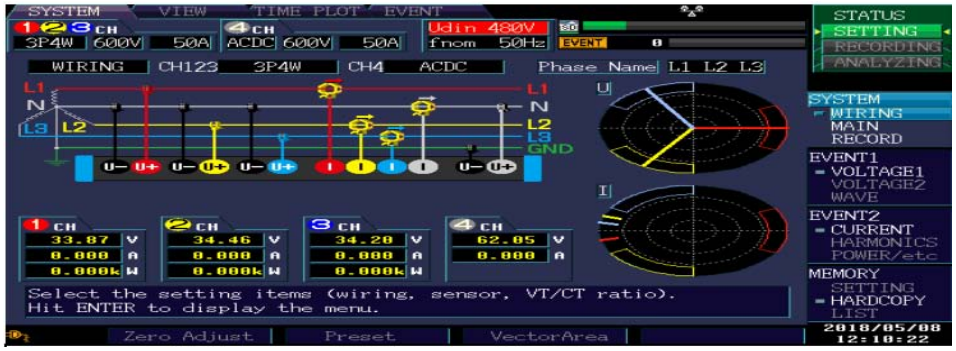

Fig. 40: Experimental results-DVR with SPWM for swell (16%) voltage with compensation

Fig. 41: Experimental results-DVR with SPWM for swell (10%) Total Harmonic Distortion (THD)

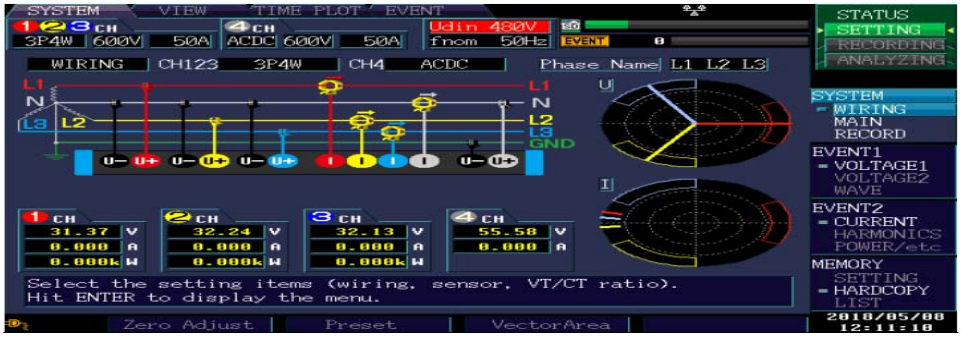

Fig. 42: Experimental results-DVR with SPWM for swell (10%) voltage without compensation

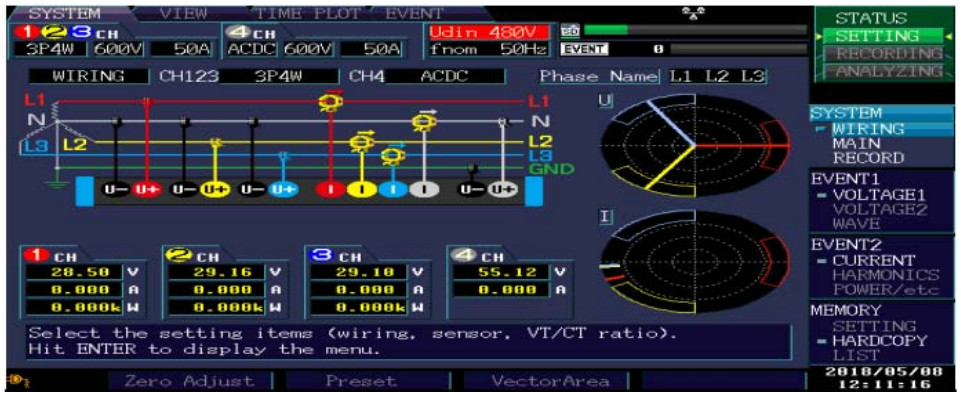

Fig. 43: Experimental results-DVR with SPWM for swell (10%) voltage with compensation

Fig. 44: Experimental results-DVR with SPWM for sag (36%) voltage without compensation

Fig. 45: Experimental results-DVR with SPWM for sag (36%) Total Harmonic Distortion (THD)

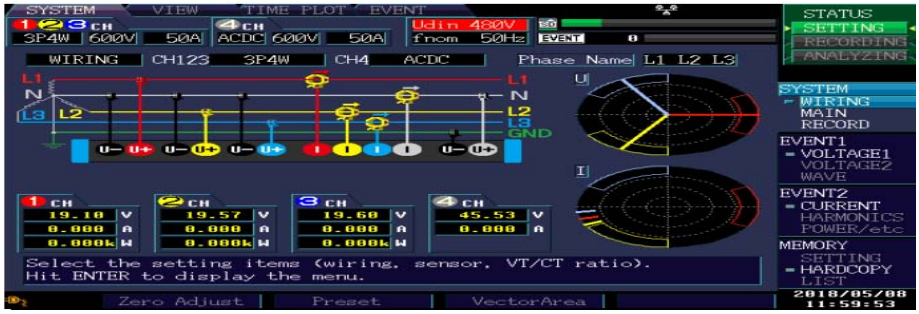

Fig. 46: Experimental results-DVR with SPWM for sag (36%) voltage with compensation

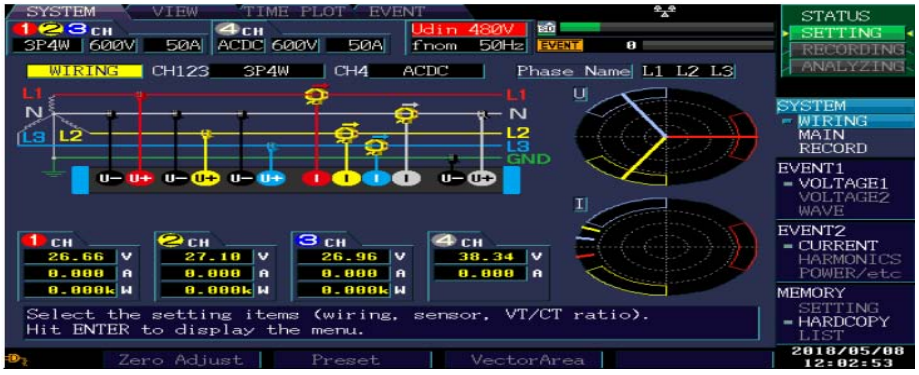

Fig. 47: Experimental results-DVR with SPWM for swell (50%) voltage without compensation

Fig. 48: Experimental results-DVR with SPWM for swell (50%) Total Harmonic Distortion (THD)

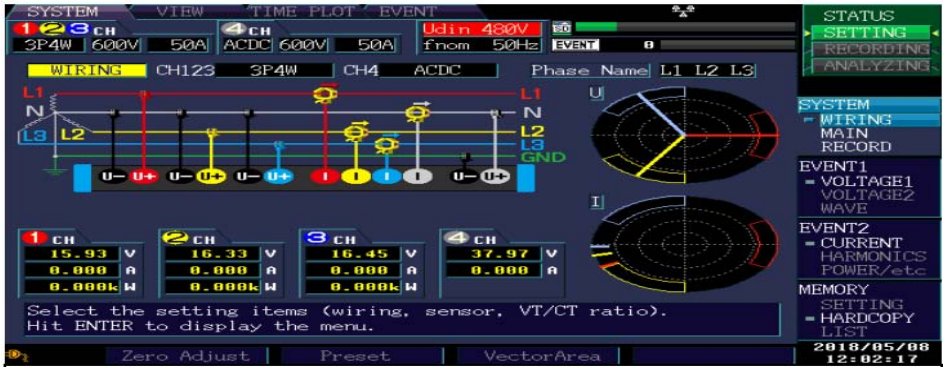

Fig. 49: Experimental results-DVR with SPWM for swell (50%) voltage with compensation

Table 5: Simulation results-sag

Sag (%)	Source voltage	Source voltage with sag	Injected voltage	Load voltage	THD
Sag					
SPWM					
10	30	27.03	4.70	30.32	3.28
25	30	22.51	9.02	30.58	5.86
35	30	19.52	10.54	29.27	5.49
50	30	22.51	9.02	30.58	4.15
3H I SPWM					
10	30	27.03	4.16	29.83	2.26
25	30	22.51	8.35	30.01	2.18
35	30	19.52	8.91	28.00	2.80
50	30	22.51	8.35	30.01	4.12
3H I PS SPWM					
10	30	27.03	4.09	29.83	1.27
25	30	22.51	8.48	30.29	2.24
35	30	19.52	8.85	28.17	2.59
50	30	22.51	8.47	30.29	3.79
Experimental result					
SPWM					
25	30	23.00	8.00	30.00	5.00
36	30	19.00	12.00	29.00	5.34
50	30	15.00	15.00	28.00	5.65

Table 6: Simulation results-swell

Sag (%)	Source voltage	Source voltage with swell	Injected voltage	Load voltage	THD
Swell					
SPWM					
10	30	33.04	4.98	28.89	2.74
25	30	37.53	6.82	30.01	3.81
35	30	40.53	12.32	28.50	3.21
50	30	37.53	6.82	30.01	3.69
3H I SPWM					
10	30	33.04	5.01	28.91	2.98
25	30	36.77	7.56	30.59	2.42
35	30	40.53	12.12	28.74	3.22
50	30	37.62	7.55	30.59	3.76
3H I PS SPWM					
10	30	33.04	5.02	28.91	1.00
25	30	37.53	7.57	30.60	1.42
35	30	40.53	12.13	28.74	2.71
50	30	37.53	7.57	30.60	3.22
Experimental result					
SPWM					
10	30	33.00	4.00	29.16	5.67
16	30	35.00	6.00	30.61	5.35
36	30	41.00	12.00	30.22	5.30

CONCLUSION

This study mainly discusses about the Power Quality (PQ) problems mitigation algorithm. The developed system is compared with existing system and is implemented by using MATLAB/Simulink algorithms. From the experimental results it is observed that, the proposed system produces accurate duration and depth of the Power Quality (PQ) problems. The proposed system is analyzed and calculated the fault for various different conditions, i.e., during fault condition in all phases and fault in individual phase and faulty condition with combinations of two phases. This study gives a complete analysis of multi-level DVR. Dynamic Voltage Restore (DVR) is considered as one of the most efficient custom power device for voltage sags and swells mitigation through simulation.

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