Journal of Engineering and Applied Sciences 14 (7): 2124-2134, 2019
ISSN: 1816-949X

Introducing Supplementary Control Scheme to DPFC During Series Converter Failure

Vikash Anand and S. K. Mallik
National Institute of Technology Patna, Department of Electrical Engineering, Patna, India

Abstract: The Distributed Power Flow Controller (DPFC) is a latest device in the FACTS family which has emerged from the UPFC and has a high reliability and relatively low cost. Two types of converters present in the DPFC are shunt and series which are connected to grids. A common DC link is present between the shunt and the series converter which is eliminated. Unlike the UPFC where in the active power exchange is through the common DC link, the active power exchange between the shunt and series converters is through the transmission line at the 3rd harmonic frequency. A high reliability of the system is provided by the redundancy of the series converters. The DPFC behaviour during the single series converter unit failure is considered is discussed in this study. In order to improve the performance of the DPFC during the failure a control scheme is proposed which is based on the principle that the single series converter failure will result into unsymmetrical current at the fundamental frequency. The series converter failure is compensated by controlling the negative and zero sequence current to zero. The control system is simulated in MATLAB environment and the results are presented to highlight the effectiveness of the proposed control scheme.

Key words: FACTS, power electronics, voltage control, internal model control, reliability, MATLAB

INTRODUCTION

In order to control the power flow in the interconnected power system network fast and reliable control schemes are needed now a days. Increasing demands for electrical energy, distributed generation and ageing of networks leads to recommending the Distributed Power Flow Controller (DPFC), providing more reliability than the other FACTS devices at low cost in a FACTS device (Yuan *et al*., 2007; Divan and Johal, 2005). Figure 1 depicts how the DPFC is derived from the UPFC in order to control the parameters in the system viz. the line impedance, transmission angle and the bus voltage magnitude (Salaet *et al*., 2004; Shinnaka, 2008; Zhang *et al*., 2002). Unlike the UPFC where in the active power exchange between the series and shunt converters takes place through a common DC link, so as to provide better control over the flow of active power in DPFC the active power exchange between the converters takes place through the transmission line at 3rd harmonic frequency (Yuan *et al*., 2007; Divan and Johal, 2005; Namho *et al*., 2001; Sozer and Torrey, 2009) by adapting the D-FACTS concept and eliminating the common DC link. In order to improve its' reliability, the DPFC utilizes multiple single phase series converters.

The cost of high voltage isolation is reduced due to the fact that the series converters can float with respect to the ground in D-FACTS (Round *et al*., 1996; Papic *et al*., 1997). This also reduces the rating of components and the cost of converter. Figure 2 depicts the DPFC in a simple two bus system.

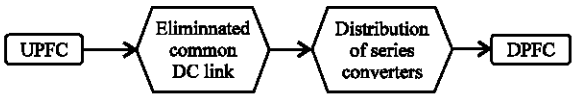

Fig. 1: Evolution of DPFC

The voltage magnitude and the active and reactive power flow can be instantly controlled by the DPFC. The DPFC can control current in each phase separately, since, it has single phased series converters. This compensates both, the negative and zero sequence unbalanced current. In the light of the above facts, this study tries to investigate the DPFC capability in balancing the network (Jamshidi *et al*., 2012; Ramya and Rajan, 2012). For this purpose, the existing DPFC controller are supplemented with additional controllers with a control principle of monitoring the negative sequences and zero sequences current through the transmission line and compelling them to be zero. The study also proposes a control scheme in order to improve the performance of the DPFC during the failure of the series converter. The control scheme design and corresponding simulation are thoroughly presented.

Corresponding Author: Vikash Anand, National Institute of Technology Patna, Department of Electrical Engineering, Patna, India

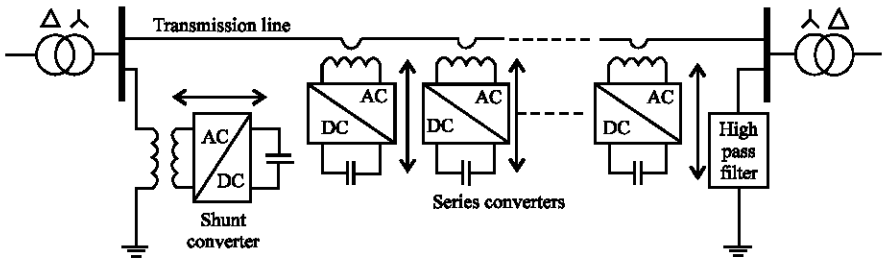

Fig. 2: Basic structure of DPFC

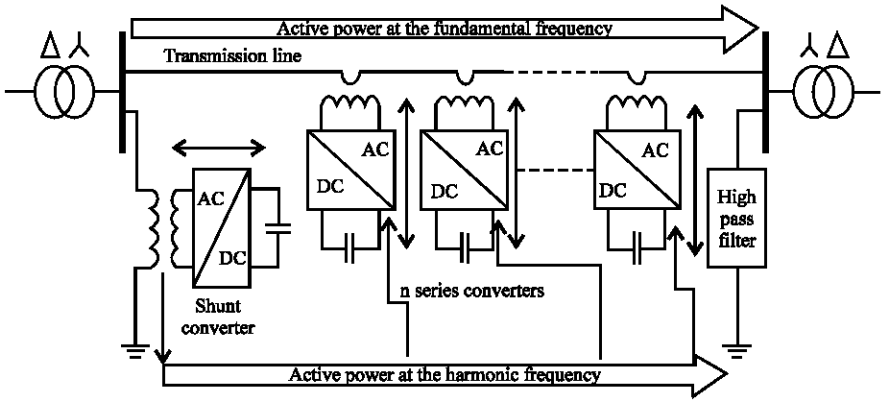

Fig. 3: Schematic diagram of DPFC

The study starts with highlighting the principle of the DPFC and its corresponding control scheme and unravels its behaviour during the failure of the series converter. Further, in order to compensate the asymmetry in the DPFC performance, the adapted control scheme is introduced in the central control unit for series converters and analysed. This control scheme i verified through MATLAB/Simulink and the results are presented towards the end of the study (Bangarraju *et al*., 2016; Nohara *et al*., 2007; Padiyar and Kulkarni, 1998).

Working principle of the DPFC: In the DPFC, one shunt and n series converters are present. Using the formula shown in Eq. 1 the value of n is selected:

$$n = \frac{\text{Total kVA rating required}}{\text{kVA rating of single DPFC unit}} \quad (1)$$

The shunt converter is similar to a STATCOM whereas the Series Converters (SSSC) employ the concept of the D-FACTS. Both, the shunt and the series converters in the DPFC are independent and have a individual DC link capacitor in order to provide the requisite DC voltage. The DPFC configuration is depicted in Fig. 3.

Any direct connection 'DC link' is not utilized for exchanging the power between the DC port of shunt and the AC port of the series converters. Transmission line is utilized by the DPFC as an inter-connection between these two converters. Its power exchange methodology depends upon the non-sinusoidal components power theory. According to the Fourier series, a non-sinusoidal component can be expressed in summation of the sinusoidal components at distinct frequencies. The active power is expressed by a product of voltage and current. The integral of a few terms with distinct frequencies are zero. The equation for active power is presented as in Eq. 2:

$$P = \sum_{i=1}^{\infty} V_i I_i \cos\varphi_i \quad (2)$$

Here, V_i and I_i represent the voltage and current of the ith harmonic frequency, respectively whereas φ_i is the angle between voltage and current at same frequency.

Since, all the components are independent in the above equation of active power in the DPFC, the shunt converter absorbs the active power in one frequency. But, its output power is generated in different frequency.

Operating principle and equivalent network of the DPFC: Figure 4 depicts the simplified circuit configuration of the DPFC placed in a two bus system's transmission line. Whilst the active power is generated by the power supply, the shunt converter absorbs the power in the fundamental frequency of current. Meanwhile, the 3rd

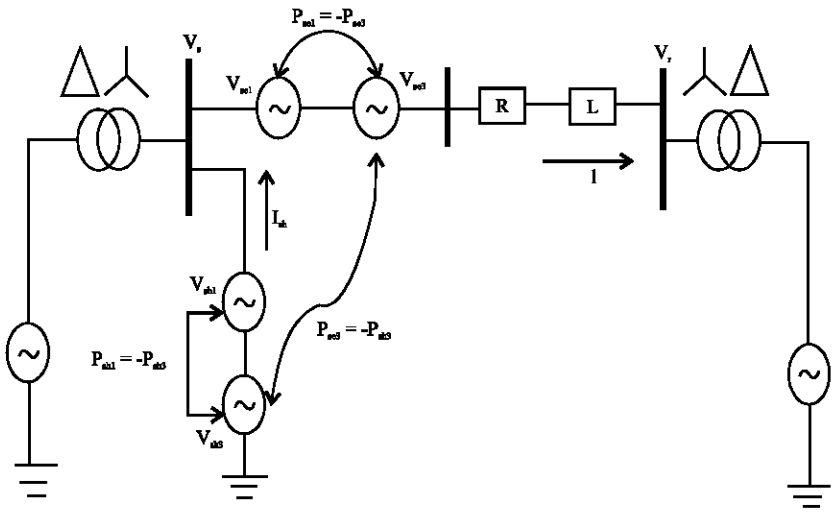

Fig. 4: Simplified network of DPFC

harmonic component gets stuck in Y-Δ transformer due to which the shunt converter's output port pushes the 3rd harmonic current into the Δ-Y neutral of the transformer. Consequently, the harmonic current circulates in the transmission line and controls the series capacitor's DC voltage.

In order to exchange the active power in the DPFC, the 3rd harmonic is selected and a high pass filter is required in order to prepare a closed loop for harmonic current. Since, the 3rd harmonic current gets stuck in the transformer's Δ winding; it eliminates the requirement of high pass filter at the system's receiving end. Hence, it can be stated that by using the 3rd harmonic concept in place of high pass filter, a cable is connected between Δ winding of the transformer and ground which routes the harmonic current to ground.

Control mechanism of the DPFC: The DPFC consists of three control module, namely, central control, shunt control and series control for the control of different converters as shown in Fig. 5.

The shunt control and the series control units act as local controllers with specific converter parameters. At the power system level, the function of the DFFC is facilitated by the central control unit.

Central control: The reference signals for shunt and series converters of the DPFC is generated by the central control which is focused on the tasks of the DPFC at the power-system level such as power-flow control, low-frequency power oscillation damping and balancing of asymmetrical components. As per the requirement of the system, the central control gives voltage-reference signals and reactive current signals for the series

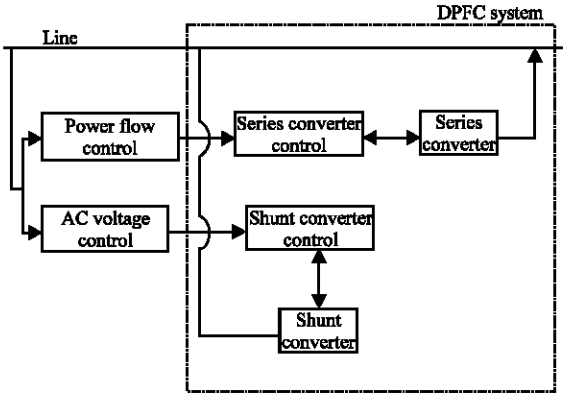

Fig. 5 Control block diagram of DPFC

converters and the shunt converters, respectively. It is worth mentioning here that all reference signals generated by the central control are at the fundamental frequency.

Power flow control: It receives the set point for power flow from the system operator and calculates the fundamental frequency voltage which should be injected by the series converters.

AC voltage control: It gives the set points to shunt converter for reactive power compensation at the fundamental frequency.

Shunt control: The shunt control aims at infusing a constant third harmonic current into the line to provide active power for the series converters. The 3rd-harmonic current is locked with the bus voltage at the fundamental frequency. Meanwhile, it maintains the capacitor DC

voltage of the shunt converter by absorbing active power from the grid at the fundamental frequency and injects required reactive current at the fundamental frequency to the grid.

Series control: Each series converter has its own series controller which is utilized to maintain the capacitor DC voltage of its own converter by utilizing the components of the 3rd harmonic frequency and to generate series voltage at the fundamental frequency needed by the central control.

MATERIALS AND METHODS

DPFC performance analysis during series converter failure: Short circuit and open circuit failures are the two types of failures occurring in the DPFC series converters. Since, short circuit does not interrupt the transmission line, it is not a big problem for the series converters. However, when an open circuit series converter leads to an open circuit transmission line which influences the whole network. A bypass circuit is provided for each series converter in order to prevent the open circuit of the series converters. A crowbar is present parallel to the output terminals of the series converter. If the series converter has an open circuit, the crowbar is connected in order to provide bypass for the transmission line. Figure 6 depicts a typical DPFC. The control objectives in the system are the $|V_1|$ and the transmission line P&Q.

Where, $|V_1|$ is controlled by the shunt device by infusing leading or lagging current into the connection point. Arrow 1 in Fig. 6 illustrates the effect.

P and Q are the system power flow which is controlled by the series device by infusing proper voltage into the transmission line. Real and reactive power is exchanged with the system by the series device. Arrow 2 in Fig. 6 depicts the reactive power which is locally exchanged with the DC capacitor bank.

The active power infused into the line by the series device is drawn from the shunt converter through the transmission line by utilizing the concept of 3rd harmonic. The 3rd harmonic current is pushed into the Δ-Y transformer's neutral by the shunt converter's output port. Consequently, the harmonic current circulates within the transmission line and controls series capacitor's DC voltage. Arrow 3 pair in Fig. 6 illustrates the real power flow.

Hence, the adapted control scheme is employed in the central control unit with an objective of controlling the negative and zero sequence current to zero during the failure of the series converter. The next study presents the principle and analysis of the adapted control scheme and corresponding revises within the power flow control loop.

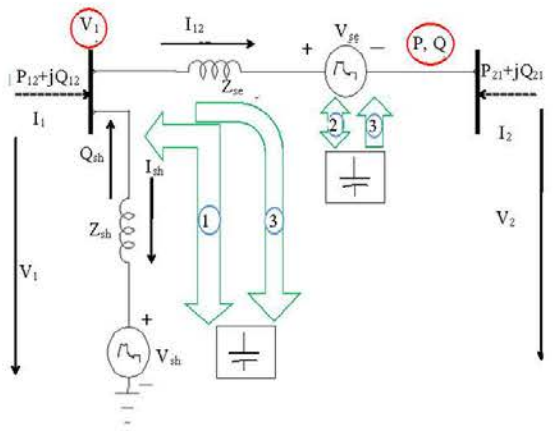

Fig. 6: Simplified circuit of DPFC during series converter failure

Mathematical analysis during the series converter failure: Assuming the DPFC is placed in a two port transmission network as shown in Fig. 7 with V_s and V_r on the sending receiving ends bus voltages, respectively. The total voltage injected by all series converters is v_{se} and the number of series converter unit per phase is N.

The failed series converter emerges as a short circuit in the transmission line stops providing desired voltages. Therefore, total voltage infused by the series converters in different phases becomes asymmetrical due to failure of series converter in phase a which is expressed in Eq. 3:

$$v_{se} = \begin{bmatrix} \frac{N-k}{N} v_{sea} \\ v_{seb} \\ v_{sec} \end{bmatrix} \quad (3)$$

where, k is the number of failed converter in phase a. The unbalanced series voltage can be represented by sequence analysis as in Eq. 4:

$$v_{se} = \begin{bmatrix} v_{se}^{+} \\ v_{se}^{-} \\ v_{se}^{0} \end{bmatrix} \quad (4)$$

The relationship between and the number of the failed converter is calculated in Eq. 5:

$$v_{se}^{-} + v_{se}^{0} = \frac{k}{N} v_{se} \quad (5)$$

This asymmetrical series voltage results into asymmetrical current in the line, resulting in a decrease in

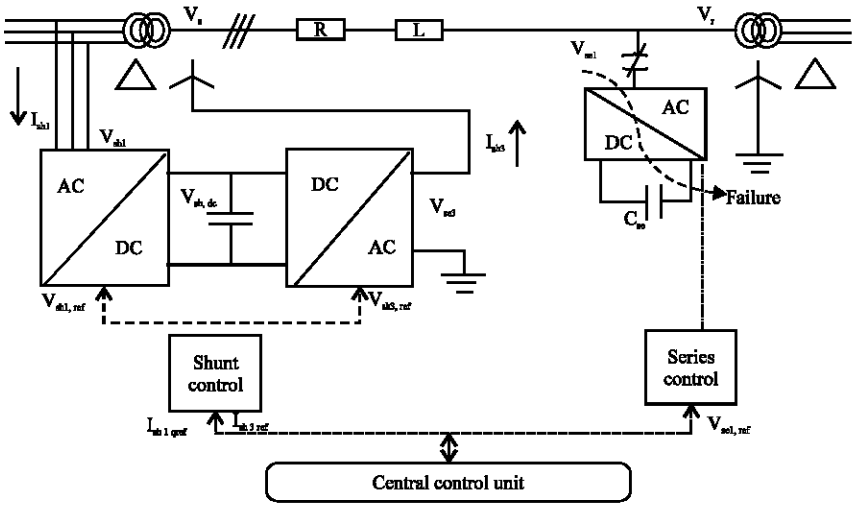

Fig. 7: Network configuration of DPFC

the network's power quality. The current at the fundamental frequency and at the 3rd harmonic frequency is influenced by the series converter failure. Equation 6 represents the unbalanced line current at the fundamental frequency:

$$\begin{bmatrix} i^{+} \\ i^{-} \\ i^{0} \end{bmatrix} = \begin{bmatrix} 1/Z^{+} & 0 & 0 \\ 0 & 1/Z^{-} & 0 \\ 0 & 0 & 1/Z^{0} \end{bmatrix} \begin{bmatrix} V_s - V_r + v_{se}^{+} \\ v_{se}^{-} \\ v_{se}^{0} \end{bmatrix} \quad (6)$$

where, Z_+, Z^- and Z_0 represents the transmission line impedance in the positive, negative and zero sequence, respectively. The line current at the fundamental frequency comprises the components of the negative and zero sequence during the failure of the single series converter unit. Their magnitudes depend on the negative sequence line impedance and zero sequence line impedance and the number of failed converters. Equation 7 presents the active power at the fundamental frequency needed by each phase:

$$\begin{bmatrix} P_{sea} \\ P_{seb} \\ P_{sec} \end{bmatrix} = \mathrm{Re}\begin{bmatrix} -V_{sea} \times I_a^{*} \\ -V_{seb} \times I_b^{*} \\ -V_{sec} \times I_c^{*} \end{bmatrix} \quad (7)$$

where, I^* complex conjugate of current at respective phases. The total active power absorbed in this phase is different from the amount of active power absorbed in other phases (without faulty converters) because a faulty series converter doesn't absorb any active power. This leads to a change in the 3rd harmonic current. This 3rd harmonic current will contain positive and negative

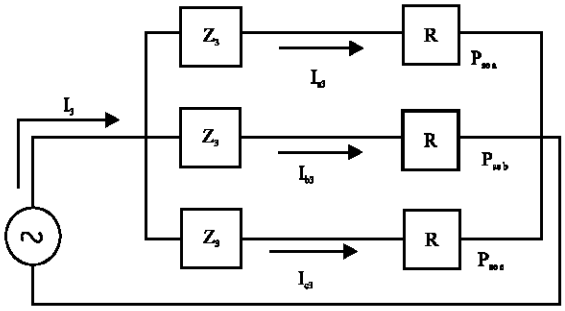

Fig. 8: Equivalent network configuration of DPFC at 3rd harmonic

components which cannot be blocked by the Y-Δ transformer. Figure 8 shows the equivalent network of the DPFC at the 3rd harmonic. Consequently, the 3rd harmonic frequency circuit can be expressed by the following Eq. 8:

$$\left.\begin{aligned} I_{a3}+I_{b3}+I_{c3} &= I_3 \\ Z_3 I_{a3}+\frac{P_{sea}}{I_{a3}^{*}} &= V_3 \\ Z_3 I_{b3}+\frac{P_{seb}}{I_{b3}^{*}} &= V_3 \\ Z_3 I_{c3}+\frac{P_{sec}}{I_{c3}^{*}} &= V_3 \end{aligned}\right\} \quad (8)$$

where in V_3 is the voltage across the transmission line. As Eq. 8 is not linear, analytical solutions for the 3rd harmonic current is difficult to achieve. However, by applying some typical DPFC parameters and solving the equations numerically, it is found that the non-zero sequence 3rd harmonic current is less than 10% of the nominal line current. In order to eliminate the asymmetry

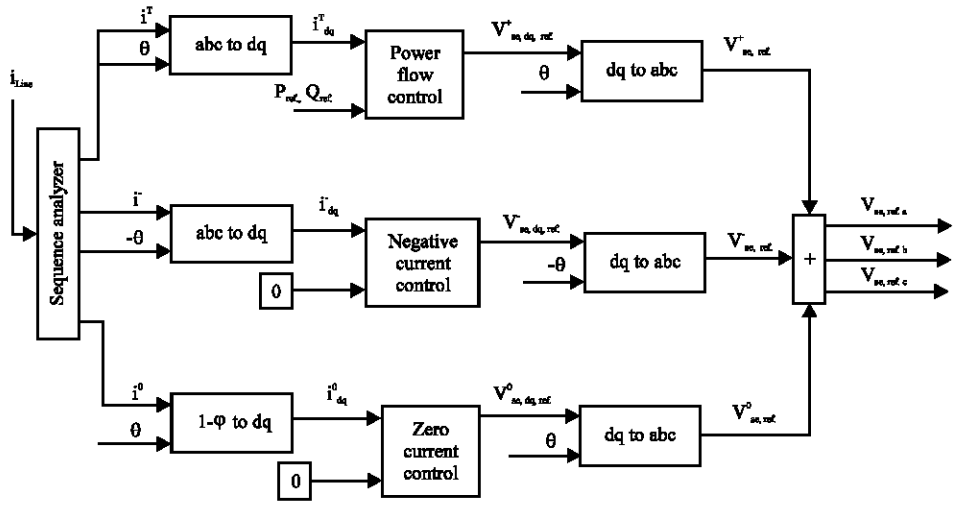

Fig. 9: Adapted control scheme in central control unit

current at the fundamental frequency and the leakage at the 3rd harmonic frequency, a supplementary control is needed to boost the infused voltage in the faulted phase.

Adapted control scheme to improve the DPFC performance: The supplementary control principle is to allow the remaining converters in line with the fault converters to inject more voltages to maintain the voltage balance between the fundamental frequency phases. As the series converters are centralizing controlled, this supplementary control is within the central controller. The supplementary control has two requirements:

- The controller should be capable of distinguishing the phase with the faulty converter and provide correct compensation voltage reference
- The communication between central control and series converters in different phases should be independent for enabling the series converters in one phase to generate different voltage from the other phases

Adapting supplementary control in central control: The basis of the proposed control scheme is that the failure of a single series converter leads to unsymmetrical current at the fundamental frequency. The failure of the series converter is automatically compensated by controlling the negative and zero sequence current to zero. Two current control loops are added to the existing DPFC controller for this purpose, so as to control zero sequence current and negative sequence current, respectively. These two supplementary controllers are positioned in the central controller. All these controllers are always functional. Figure 9 shows the control scheme of the central control with these supplementary controllers.

The sequence analyser processes the three-phase line current first. For power flow control purposes the positive sequence current is used and for series converter failure compensation other sequence currents are used. The negative and zero sequence current is zero when there is no failed series converter. The two current controllers force the negative and zero sequence current to become zero in the case of failure of the series converter. In order to construct the reference signals for the series converters in different phases the voltages created by the two controllers are added with the positive voltage.

The proposed method measures the fundamental frequency voltages at the sending and receiving ends (V_s and V_r) and the current through the line I. According to the measured information, the total voltage injected by all series converters $v_{se\ 1\ cal}$ can be calculated by the following Eq. 9:

$$v_{selcal.} = V_s - V_r - IZ \quad (9)$$

Here, voltage and current are column vectors consisting of the three phase information whereas Z is the line impedance at the fundamental frequency. The operational status of the series converters can be known by comparing this calculated voltage along with the total reference voltage which is generated by the central control. Equation 10 shows one or more faulty converters in that phase:

$$v_{selcal.} < v_{selref.} \quad (10)$$

Supplementary control for series converter reference: A controller is applied between the central control which

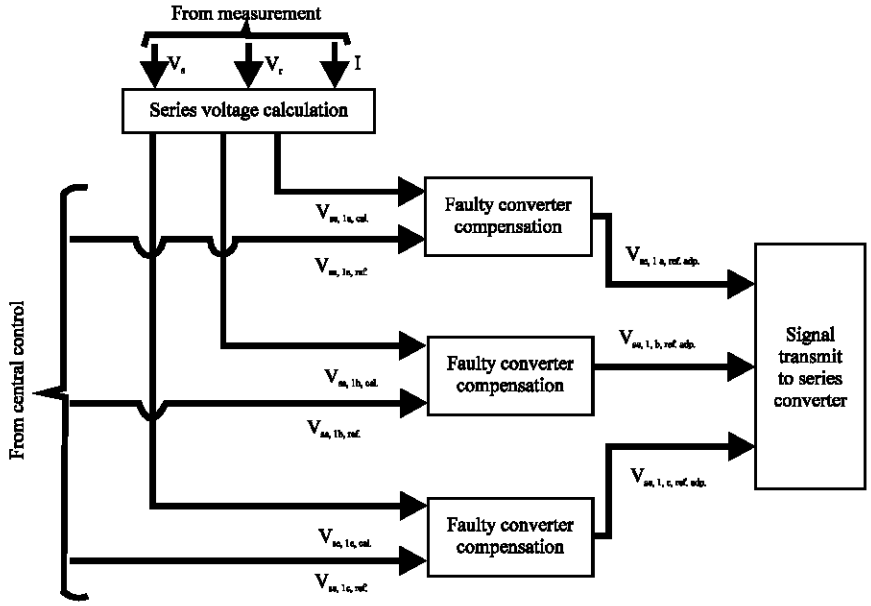

Fig. 10: Adapted control scheme for series control unit

provides the total reference voltage and the signal transmitting device which sends the reference to each series converter in order to compensate for the missing voltage brought about by the faulty converter. This controller generates a modified voltage reference for each series converter as per the calculated operation status of the series converters. Since, the series converters in different phases are independently controlled, three supplementary controllers are required which is depicted in Fig. 10.

The compensation controller's objective is the generation of the adapted reference signal according to the series converters' operation status. The reference voltage v_{selcal} and the calculated voltage v_{selref} are the input signals of the controller. The reference voltage of a single series converter $v_{se\ 1\ ref.adp.}$ is the output signal. Since, the reference voltages for series converters are in DC quantities, two independent controllers are required for one phase which is responsible for the d and q components, respectively. Six controllers are needed in total for the compensation of the faulty series converter. Due to the identity of each controller, the design of one controller will be introduced only.

Analysis of supplementary controller: As shown in Figure 11 the compensation controller is a close loop control with $v_{se\ 1\ ref}$ as the reference, $v_{se\ 1\ cal}$ as the feedback and $v_{se\ 1\ ref.adp.}$ as the output. In order to limit the output of the controller saturation block is added.

As expressed in Eq. 11 the open loop transfer function G (s) from $v_{se\ 1\ ref.adp.}$ to $v_{se\ 1\ cal.}$ should be found first for designing the controller, theoretically:

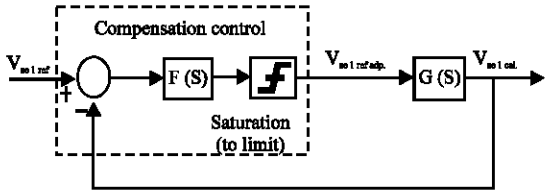

Fig. 11: Unbalanced control scheme of series converter

$$v_{selcal.} = N \times v_{selref.adp.} \quad (11)$$

where, N is the number of series converters per phase. However, there will be a delay between the two components due to the measurement and the response time of series converter control. For simplification purpose this delay is assumed to be a first order system, then the transfer function from $v_{se\ 1\ ref.adp.}$ to $v_{se\ 1\ cal.}$ can be presented as Eq. 12:

$$G(s) = \frac{v_{selcal.}}{v_{selref.\ adp.}} = n\frac{1}{sT_r+1} \quad (12)$$

Where:

n = (N-k) = The number of active series converters
T_r = The rise time of the delay

Within the transfer function, n is a variable value and should be considered as a disturbance. According to the delay of the measurements and the control of series converters, 0.01 sec. is recommended for the constant T_r. Equation 13 shows the method to calculate the parameters of the controller function according to the Internal Model Control (IMC) method:

$$F(s) = \frac{\alpha}{s} G(s)^{-1} \quad (13)$$

where, α is the design parameter which provides the bandwidth of the control. The relationship between the bandwidth and the rise time (from 10-90% of the final value) is $\alpha = \ln 9/T_r$. Since, G (s) is a first order system, the control is a PI with parameters as shown in Eq. 14:

$$k_p = \frac{\alpha T_r}{n}, k_i = \frac{\alpha}{n} \quad (14)$$

n is the number of installed active series converter unit per phase within the parameters.

RESULTS AND DISCUSSION

MATLAB/Simulink has been used for simulation. The DPFC is tested in a two bus system where in two fixed sources of voltage are linked to the transformers to signify the infinite buses. In order to simplify the calculation, two sets of three 1-ϕ series converter are connected to control the power flow through the line as shown in Fig. 12. Table 1 lists the selected system parameters for this model.

At the fundamental frequency each series converter generated 0.02 pu voltage. In phase a one of the series converter is short circuited manually at t = 1 sec. The performance of the supplementary control is demonstrated by keeping the compensation controllers off before t = 1.5 sec. The system behaviour is presented with and without the supplementary control.

Figure 13 and 14 shows how without the controller the 3-ϕ system becomes asymmetrical during the failure of the series converter. The phase difference caused by the series converter failure is successfully compensated by the supplementary controller. Since, one converter has a fault in phase a, hence, phase a control signal should be more than twice larger without the fault while the other phases control signals should remain unchanged. Figure 15 and 16 depicts the magnitude of the series converter reference voltage and magnitude of the voltage infused by all the series converters, respectively.

In case of failed one converter the ability of infusing a controllable series voltage is represented by the supplementary control present at the series converter. The active and reactive power can be independently controlled as shown in Fig. 17 indicating that the supplementary control at the fundamental frequency is

Table 1: MATLAB/Simulink system parameters

Parameters	Values
V_s (pu)	1
V_r (pu)	1
θ (^{0})	1.2
X (pu	0.25
$I_{3,ref.}$ (Pu)	1
$V_{se,dc,ref.}$ (pu)	0.09
$V_{sh,dc,ref.}$ (pu)	0.2
C_{se} (μF)	2200
C_{sh} (μF)	6600

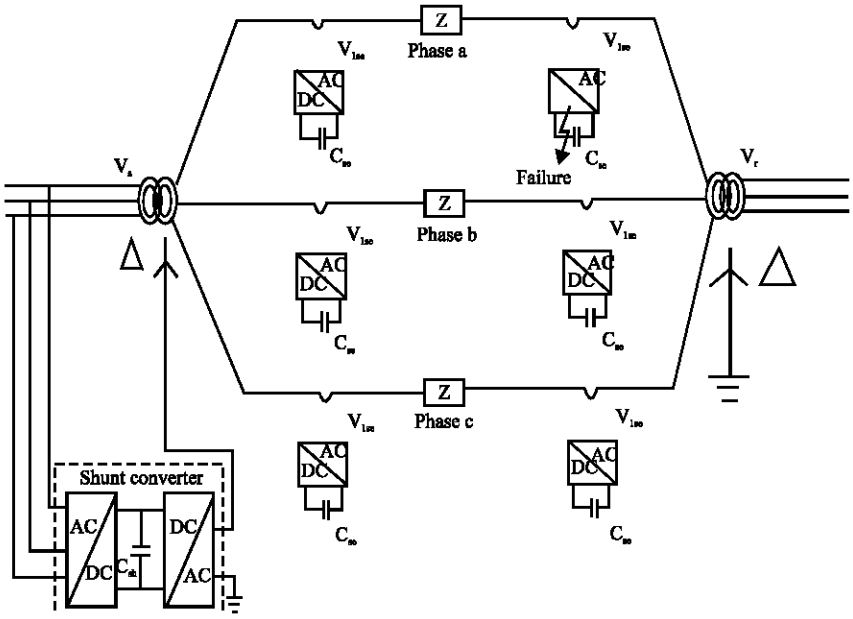

Fig. 12: Network of DPFC MATLAB/Simulink setup

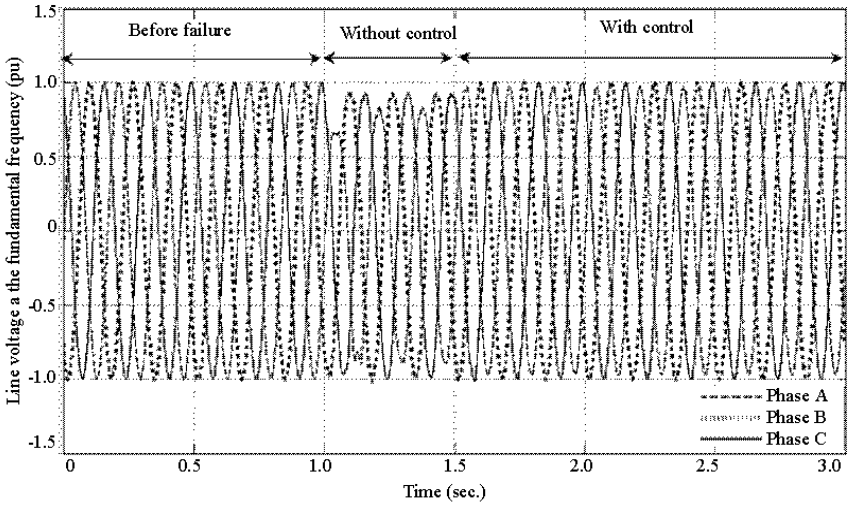

Fig. 13: The waveform of three phase voltage at the fundamental frequency

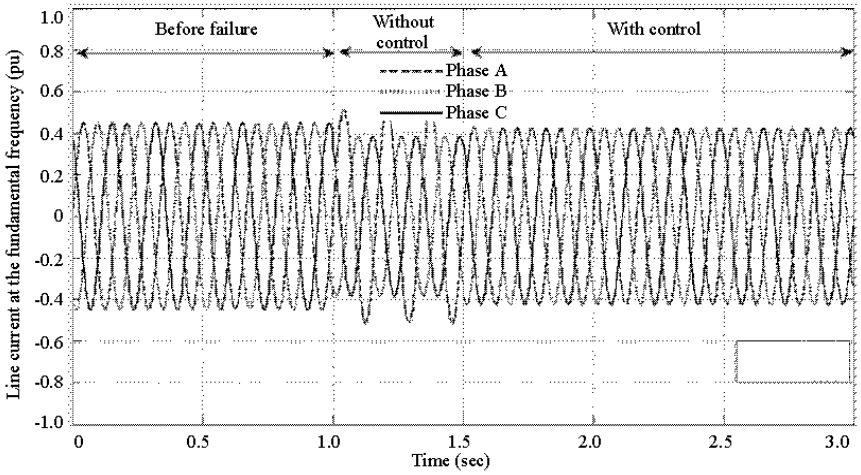

Fig. 14: The waveform of line current at the delta side of transformer

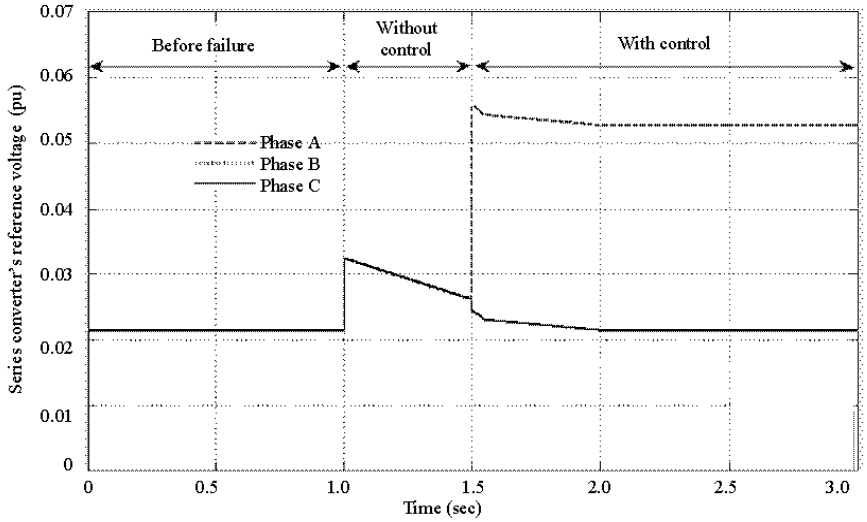

Fig. 15: The reference voltage magnitude of series converter

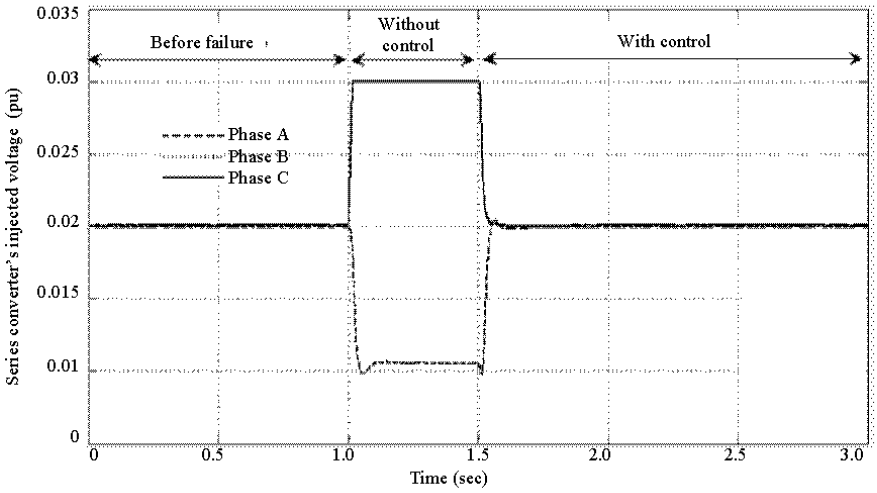

Fig. 16: The injected voltage magnitude of series converters

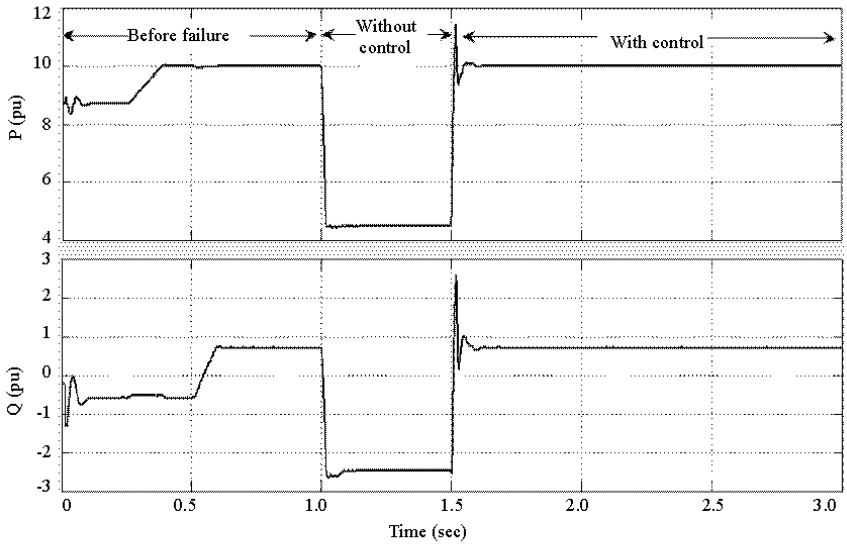

Fig. 17: The waveform of active and reactive power flow

capable of infusing the controllable voltage. The variation in the DC voltages of the series converters causes the transients.

The simulated results of DPFC prove that on applying the supplementary control scheme in MATLAB/Simulink the asymmetry caused by one series converter failure could be completely compensated.

CONCLUSION

The present study analyses the DPFC performance before and during the failure of a single series converter unit. At the secondary side of the single-turn transformer the series converters have over-voltage protection due to which the failed series converter appears short-circuit to the transmission line and the voltage infusion between phases is unbalanced. The power network becomes asymmetric because of this unbalance resulting in unsymmetrical current at the fundamental frequency. The 3rd harmonic current which used to be zero sequence consists of positive and negative components, thus, leaking to rest of the networks. In order to improve the performance of the DPFC during the failure of the series converter, a supplementary control scheme is proposed to adapt in the DPFC central control unit which is based on the principle of monitoring the line current's zero and negative sequence components and control them to be zero. The control scheme has been simulated in MATLAB

and it is proven that the asymmetry resulting from the failure of the series converter can be compensated completely.

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