Journal of Engineering and Applied Sciences 14 (12): 4060-4066, 2019
ISSN: 1816-949X
© Medwell Journals, 2019

Biomedical ECG Signal Enhancement via. CMOS Spectrum

[1]S.M. Abdul Gaffar, [2]Kadim Karim Mohsen and [1]Satar Habib Mnaathr
[1]Department of Electrical and Electronic Engineering,
[2]Department of Mechanical Engineering, Engineering College, University of Thi-Qar, Nasiriya, Iraq

Abstract: The commotion execution of the CMOS operation amp. Assumes a crucial part in immense zone of use for example, biomedical, media transmission and so on. To test the activity of the proposed CMOS operation amp Electrocardiogram (ECG) signals utilized as information signals of the shut circle voltage pick up with 2 mV top to top esteem and 250 Hz recurrence. This frail signals was increased to 330, 225 and 42 mV utilizing two-arrange CMOS operation amp, pseudo CMOS operation amp and collapsed course operation amp individually. They got reenactment result concurred with the hypothetical figurings two phase CMOS operation amp with inner biasing current circuit was proposed to understand the primary sort of the CMOS operation amp, the second plan in view of pseudo CMOS operation amp method and the last strategy utilized as a part of the proposed operation amp was a solitary collapsed course CMOS operation amp.

Key words: Biomedical signals, electroencephalogram signal, CMOS, ECG, hypothetical, reenactment

INTRODUCTION

Biomedical signals, for example, Electrocardiogram (ECG) play play increasingly imperative part in the determination and treatment for different sicknesses. ECG signals have the qualities of low abundancy and low recurrence. The signals data transmission of ECG seethes from 0.1-150 Hz with signals sufficiency under 8 mV. So, these signals require fastidious planning of the securing and recording units for catching and putting away these signals. A low commotion, low voltage and low power utilization enhancer is one of the key circuits for recognizing these little level signals in the versatile ECG recording framework under battery control. A speaker executed in CMOS innovation is alluring because of its low utilization ability, thick mix and minimal effort. Not with standing in CMOS innovation 1/f clamor turns into a significant issue which restrains the base distinguishable signals in enhancer at low recurrence (Cao *et al*., 2017; Ng *et al*., 2018; Sarma *et al*., 2017; Lim and Flynn, 2015; Jana *et al*., 2018; Chen *et al*., 2018).

Theory of electroencephalogram signal: An average ECG checking framework comprises of A simple Front-end speaker (AFE) to give introductory pick up and decrease the impact of commotion in the accompanying stages; a low-pass channel to dismiss clamor at frequencies over the data transfer capacity of ECG signals a variable pick up enhancer to bring the signals inside the dynamic scope of the simple to Advanced Converter (ADC) and a Nyquist ADC which tests the ECG motion at a rate of no less than twice its transmission capacity. The subsequent inspected signals would then be able to be prepared with an advanced Signal Processor (DSP) and either put away in memory or remotely transmitted to an outer apparatus (De *et al*., 2018; Nakai, 2018; Sobreviela *et al*. 2017). Biomedical signals, for example, Electrocardiogram (ECG), Electromyogram (EMG), Electroencephalogm (EEG) are portrayed by their low voltage-levels and low recurrence, Table 1 demonstrates the qualities of these signals (Sobreviela *et al*., 2017; Moulahcene *et al*., 2014) (Fig. 1).

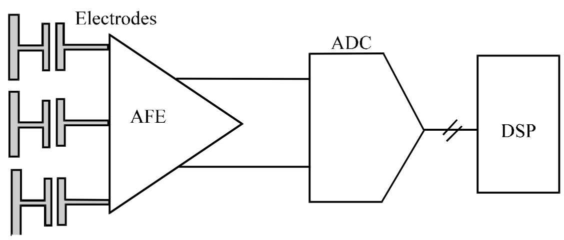

Fig. 1: Block diagram of ECG

Table 1: Most commonly used biomedical signals

Signals	Frequency	Amplitude
ECG	0.05-250 Hz	5 uV-8 mV
EEG	0.5-200 Hz	2-200 µV
EMG	0.01-10 kHz	50 uV-10 mV

Corresponding Author: S.M. Abdul Gaffar, Department of Electrical and Electronic Engineering, Engineering College, University of Thi-Qar, Nasiriya, Iraq

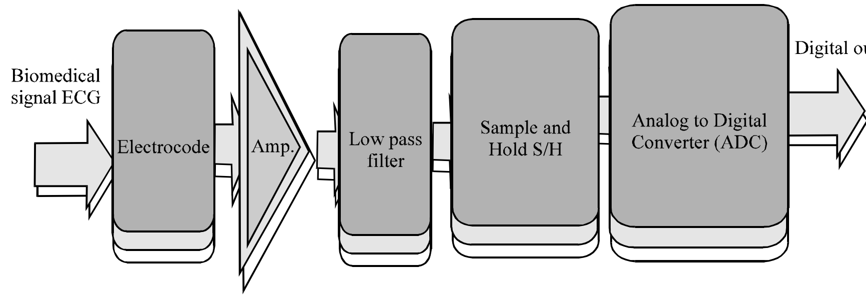

Fig. 2: Proposed ECG data acquistion

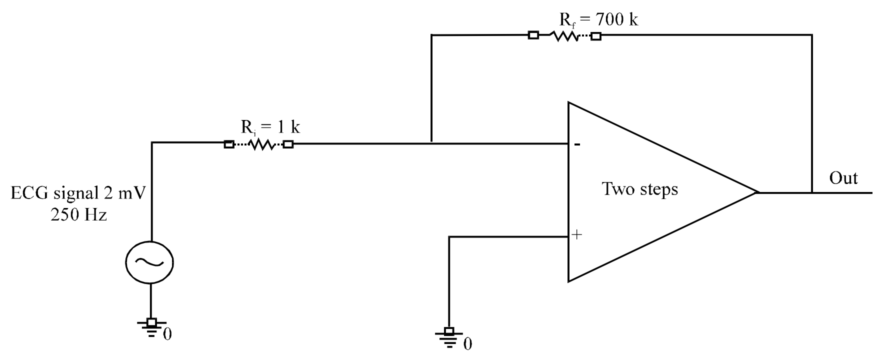

Fig. 3: Block diagram of the proposed two stages CMOS op-amp

MATERIALS AND METHODS

ECG data acquisition systems: The ECG signals that obtained is in the scope of 5 μV-8 mV. Because of the frail voltage level, the signals are sustained into an enhancer circuit to be opened up to an alluring voltage level. Yield from the intensifier is then sustained into a bandpass channel circuit and a high Q step channel. The reason for this sifts is to channel through the simple low and high recurrence clamor segments of the signs and the 60 Hz control line impedance. The alluring simple yield from the channel is then sent to S/H and ADC to end up a computerized signal. From that point onward, these computerized information being handled in PCs or chip. Figure 2 demonstrates the proposed ECG information procurement framework (Gray *et al*., 2017).

The proposed two stage CMOS op-amp based ECG signal: The square outline of the proposed two phase CMOS operation amp utilized as shut circle speaker for ECG signal is appeared in Fig. 3 and 4 with criticism resistor and info resistor 200 and 1 kμ, separately. Table 2 and 3 represents the door measurements of the MOSFET transistor of the propoesd two phase CMOS operations amp utilizung 100 μA baising current approach.

Table 2: Specifications of the CMOS op-amp using 100 μA biasing current approach

Specifications	Values with units
DC gain	70 dB
Gain bandwidth	15 MHz
Slew rate	10 V/μ sec
Supply Voltage (V_{DD}, V_{SS})	±1.8 V
Input common mod range	-1 to 1V
Phase margin	.45°
Load capacitor	10 pF

Table 3: Gate dimensions of the mosfet transistor of the proposed two stage CMOS op-amp using 100 μA biasing current

Transistor number	Types	Gate width (μm)	Channel length (μm)
M1, M2	N	4.680	0.18
M3, M4	P	0.390	0.18
M5, M8	N	0.977	0.18
M6	P	3.923	0.18
M7	N	4.986	0.18

The plan condition of two phase CMOS operation amp with 100 μA is given in condition (Varghese and Joseph, 2018).

Steps of two-stage op-amp design

Step 1: Calculate the minimum value of compensation capacitor (c.) which is given by Gray *et al*. (2017):

$$C_c > (2.0/10)C_L \quad (1)$$

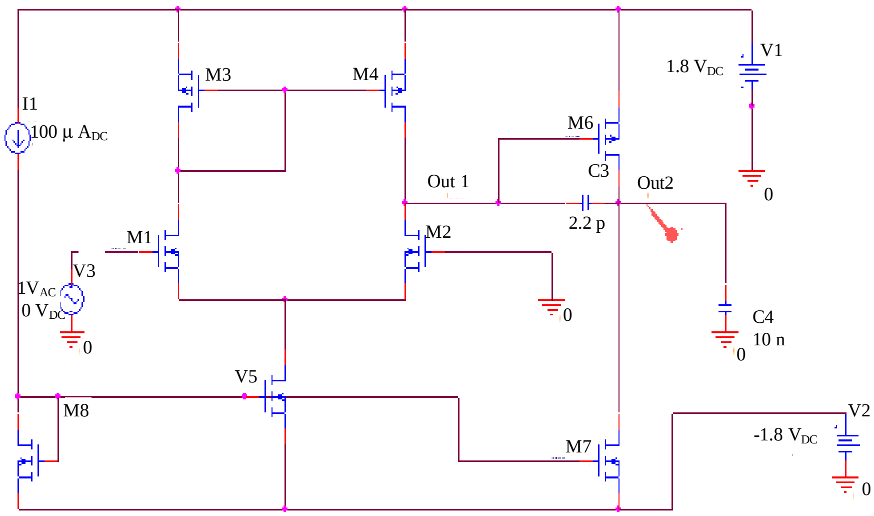

Fig. 4: Schmatic of two stage CMOS op-amp using 00 µA baising current

Step 2: Calculate current value I.:

$$I_5 = (\text{Slewrate}) * C_c \quad (2)$$

Step 3: Calculate g..:

$$g_{m1} = GBW * C_c \quad (3)$$

So,

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K_n I_1} \quad (4)$$

$$\text{Were}: I_1 = 0.5I_5 \quad (5)$$

Step 4: Calculate (W/L). using ICMR requirement, i.e.:

$$(W/L)_3 = \frac{2I_3}{kp[V_{DD}\text{-ICMR}(+)\text{-}|V_{th3}|+V_{th1}(\min)]} \quad (6)$$

Where:

$$I_3 = 0.5I_5 \quad (7)$$

Step 5: Now calculate:

$$V_{DSS} = V_{in(\min)} - V_{ss} - \sqrt{\frac{I_5}{\beta_3}} + V_{t1(\max)} \quad (8)$$

Using V.. calculate (W/L).:

$$(W/L)_5 = \frac{I5}{0.5k_n(V_{DSS})^2} \quad (9)$$

Where:

$$\beta = K(W/L) \quad (10)$$

Step 6: Calculate (W/L).:

$$(W/L)_6 = \frac{g \leq^2_{m6}}{2k_p I_6} \quad (11)$$

$$g_{m6} \geq 10g_{m4} \quad (12)$$

$$g_{m4} = \sqrt{2Kp\left(\frac{W}{L}\right)4I_4} \quad (13)$$

Step 7: Calculate (W/L).:

$$(W/L)_7 = (W/L)5 * \frac{17}{15} \quad (14)$$

Step 8: Calculate the overall gain Av:

$$A = \frac{2(g_{m2})*(g_{m6})}{I_5(\lambda 2+\lambda 4)+I_6(\lambda 6+\lambda 7)} \quad (15)$$

Simulation results: ECG motion with greatness of (2 mV) p.p voltage and 250 Hz recurrence appeared in Fig. 5. This signals utilized as contribution of the proposed two phase CMOS to test its activity and the ECG signals is acquired from the Pspice program (VSTIM source).

Figure 6 demonstrates the yield waveform of the proposed two phase CMOS operation amp. It can be seen that the estimation of ECG signals is opened up by 175 times of the information ECG motion without mutilation and the signals is reversed by straight forward

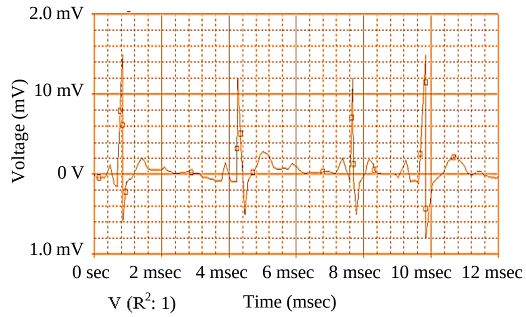

Fig. 5: ECG signal as input of CMOS op-amp

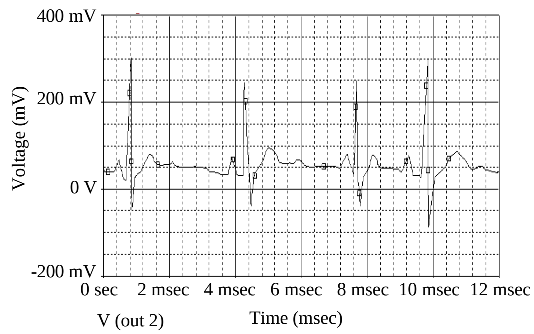

Fig. 6: ECG signal as output of two stages CMOS op-amp

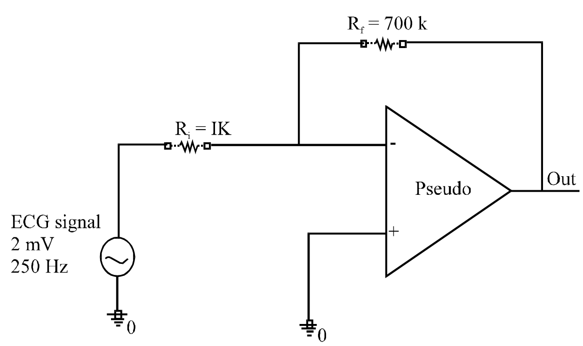

Fig. 7: Block diagram of the proposed pseucode CMOS op-amp

inverter to watch the enhancement intently. These outcomes because of the low commotion and high DC pick up execution of the proposed two phase operation amp.

The proposed pseudo cmos op-amp based ECG signal: The graph of the proposed pseudo CMOS operation amp utilized as shut circle enhancer for ECG signals is appeared in Fig. 7 with criticism resistor and info resistor are 700 and 1 kμ individually. We determine gate dimension of proposed pseudo at 100 μA in Table 5 by Eq. 13 and 14:

$$I_D = 0.5K_n\left(\frac{W}{L}\right)(V_{GS}-V_T)^2 \qquad (16)$$

$$K_n = \mu_n C_{ox} \qquad (17)$$

Where:

I_D = DC drain current
K_n = NMOS transistor transconductance parameter (K_p for PMOS)
V_{GS} = DC gate to source Voltage
V_T = Threshold Voltage
μ_n = Electron mobility (for NMOS transistor)
C_{ox} = Gate oxide Capacitance per unit area

RESULTS AND DISCUSSION

ECG signal with greatness of (2 mV) p.p voltage and 250 Hz recurrence appeared in Fig. 8 and 9. This signals utilized as contribution of the proposed pseudo CMOS to test its activity. Figure 10 demonstrates the yield waveform of the proposed pseudo CMOS operation amp. It can be seen that the estimation of ECG signals is opened up by 112.5 times of the information ECG motion without twisting. These outcomes because of the low commotion and high dc pick up execution of the proposed pseudo operation amp.

The proposed folded cascade CMOS op-amp based ECG signal: The chart of the proposed collapsed cascode CMOS operation amp utilized as shut circle intensifier for ECG signals is appeared in Fig. 11 with criticism resistor and information resistor 500 and 1 kμ separately. The gate measurements of the proposed collapsed cascode CMOS operation amp is appeared in Table 6 and 7 where we decide entryway measurement of proposed collapsed cascode at 100 μA by condition 2.16 and 2.17.

Simulation results: ECG wave with extent of (2 mV) p.p voltage and 250 Hz recurrence appeared in Fig. 13. This signals utilized as contribution of the proposed collapsed cascode CMOS to test its task. Figure 14 demonstrates the yield waveform of the proposed collapsed cascode CMOS operation amp. We would that be able to the estimation of ECG signals is opened up by 21 times of the information ECG motion without bending. This outcome because of the low clamor and high DC pick up execution of the proposed collapsed cascode operation amp.

Table 8 shows the extent estimations of the three kinds of plan, two phase, pseudo and collapsed course.

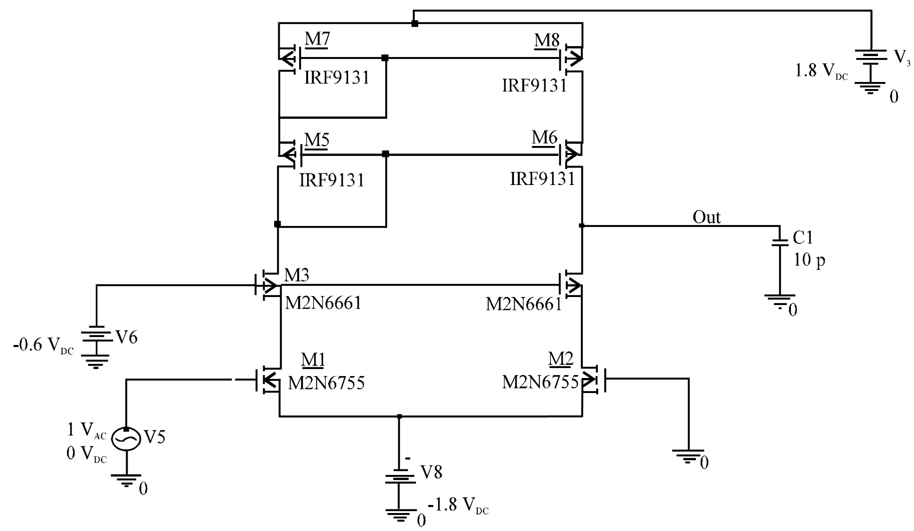

Fig. 8: Schematic of pseucode CMOS op-amp

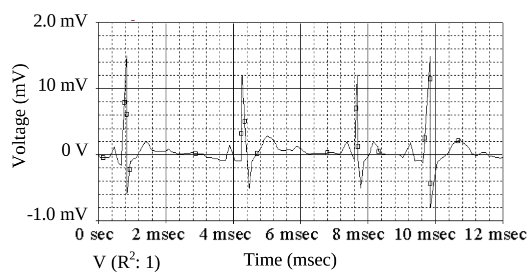

Fig. 9: ECG signal as input of CMOS op-amp

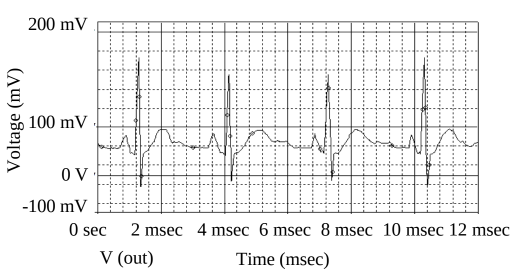

Fig. 10: ECG signal as output of pseudo CMOS op-amp

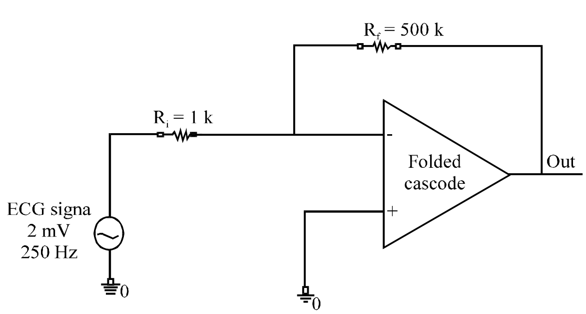

Fig. 11: Block diagram of the proposed folded cascode CMOS op-amp

Table 5: Summarized gate dimensions of mosfet of proposed pseudo at 100 μA biasing current

Transistor number	Types	Gate width (μm)	Channel length (μm)
M1, M2	N	0.06	0.18
M3, M4	N	0.03	0.18
M5, M6, M7, M8	P	0.27	0.18

Table 6: Specifications of proposed folded cascode cmos op-amp with 100 μA biasing current

Specifications	Values with unit
DC gain	70 dB
Gain bandwidth	5 MHz
Slew rate	10 V/μ sec
Supply Voltage (V_{DD}, V_{SS})	±1.8 V
Input common mod range	-1 to 1V
Phase margin	.45°
Load capacitor	10 pF

Table 7: Summarized gate dimensions of MOSFET of proposed folded cascode at 100 μA

Transistor number	Types	Gate width (μm)	Channel length (μm)
M1, M2	P	2.70	0.18
M3	P	1.95	0.18
M4, M5	N	0.58	0.18
M6, M7	N	0.58	0.18
M8, M9, M10, M11	P	2.70	0.18

Table 8: The amplification performance of the three types of CMOS Op-amp with input ECG signal (2 mV p.p)

The magnitude of ECG signal	CMOS two stage op-amp	CMOS pseudo op-amp	CMOS folded cascade op-amp
Output ECG signal (mV)	350	225	42

These qualities demonstrate the opened up ECG motion by 175 times for first sort, 112.5 times for second kinds and 21 times for third kinds. We watch that the better enhancement with low commotion is done by first sort (two phase CMOS operation amp). When we

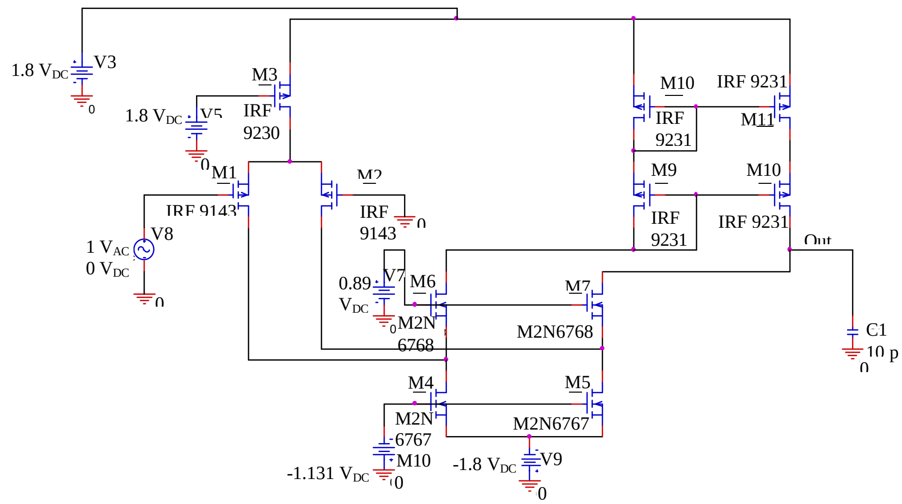

Fig. 12: Schmatic of folded cascode CMOS op-amp

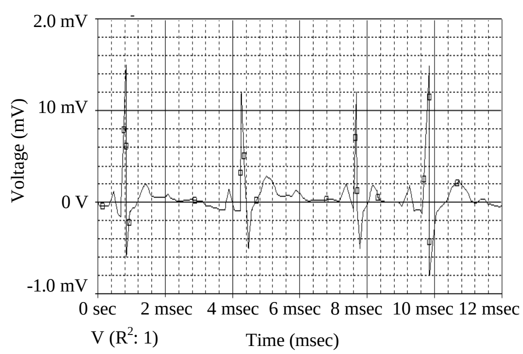

Fig. 13: ECG signal as input of CMOS op-amp

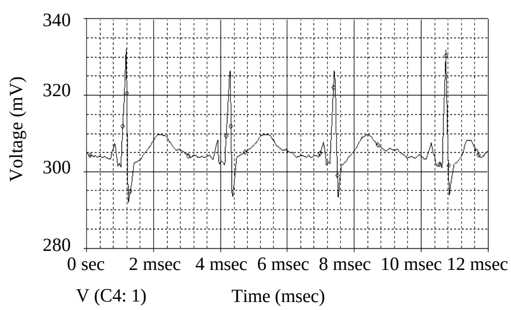

Fig. 14: ECG signal as output of folded cascode CMOS Op-amp

endeavored to extend the signals in the collapsed course saw that the commotion is expanding a direct result of the quantity of transistors many, accordingly clamor be higher.

CONCLUSION

CMOS operation amp with low info alluded voltage clamor, low Power Spectral Density (PSD), high voltage pick up and wide pick up data transfer capacity item GBW(>1 MHz) is still test the analysts, due to the elements like commotion associating and charge infusion. The proposed planned of CMOS operational speakers are tried utilizing biomedical application (ECG motion) with 2 mV and 200 Hz recurrence. ECG signals are utilized as contribution of shut circle voltage pick up circuit theses signals are opened up effectively to the worthy range without bending. The qualities demonstrate the opened up ECG motion by 175 times for first kind, 112.5 times for second sorts and 21 times for third sorts. We watch that the better enhancement with low commotion is completed by first sort (two phase CMOS operation amp). When we attempted to augment the signals in the collapsed course saw that the clamor is expanding a direct result of the quantity of transistors many in this manner commotion be higher.

ACKNOWLEDGEMENT

The researchers wish to thank the Department of Mechanical and Electrical and Electronic Engineering at Engineering College, University of Thi-Qar for its support.

REFERENCES

Cao, X., M. Zhang and C. Zhang, 2017. Design of a high flexible block-based computational CMOS image sensor. Proceedings of the 2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC), October 18-20, 2017, IEEE, Hsinchu, Taiwan, ISBN:978-1-5386-2908-6, pp: 1-2.

Chen, P.W., C.W. Huang and C.Y. Wu, 2018. An 1.97 μ, W/Ch 65nm-CMOS 8-channel analog front-end acquisition circuit with fast-settling hybrid DC servo loop for EEG monitoring. Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 27-30, 2018, IEEE, Florence, Italy, ISBN:978-1-5386-4882-7, pp: 1-5.

De, B.P., K.B. Maji, R. Kar, D. Mandal and S.P. Ghoshal, 2018. Design of optimal CMOS analog amplifier circuits using a hybrid evolutionary optimization technique. J. Circuits Syst. Comput., 27: 1-23.

Gray, P.R., P.J. Hurst, S.H. Lewis and R.G. Meyer, 2017. Analysis and Design of Analog Integrated Circuits. 5th Edn., University of Oslo, Oslo, Norway,.

Jana, D., S. Ghosh, R. RSSM. S. Mandal and A.K. Mal, 2018. Design of Low-Noise Amplifier with High CMRR for Sensor Application. In: Advanced Computational and Communication Paradigms, Bhattacharyya, S., T. Gandhi, K. Sharma and P. Dutta (Eds.). Springer, Singapore, ISBN:978-981-10-8239-9, pp: 1-10.

Lim, Y. and M.P. Flynn, 2015. A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC. IEEE. J. Solid State Circuits, 50: 2901-2911.

Moulahcene, F., N.E. Bouguechal and Y. Belhadji, 2014. A low power low noise chopper-stabilized two-stage operational amplifier for portable bio-potential acquisition systems using 90 nm technology. Intl. J. Hybrid Inf. Technol., 7: 16-19.

Nakai, T., 2018. Operational amplifier circuit and bias current supply method. Patent and Trademark Office, Washington, DC., USA. https://patents.google.com/patent/US20170040949A1/en

Ng, K.A., Y.P. Xu, Y.E.N. Shih-Cheng and N.V. Thakor, 2018. Multi-channel neural signal amplifier system providing high CMRR across an extended frequency range. Patent and Trademark Office, Washington, DC., USA. https: //patents. google. com/ patent/ US9867574B2/en

Sarma, M.P., N. Kalita and N.E. Mastorakis, 2017. Design of an low power miller compensated two stage OP-AMP using 45 nm technology for high data rate communication. Proceedings of the 2017 4th International Conference on Signal Processing and Integrated Networks (S PIN), February 2-3, 2017, IEEE, Noida, India, ISBN:978-1-5090-2798-9, pp: 463-467.

Sobreviela, G., M. Riverola, F. Torres, A. Uranga and N. Barniol, 2017. Optimization of the close-to-carrier phase noise in a CMOS-MEMS oscillator using a phase tunable sustaining-amplifier. IEEE. Trans. Ultrason. Ferroelectr. Freq. Control, 64: 888-897.

Varghese, M.M. and K. Joseph, 2018. Design of low voltage two stage CMOS operational amplifier. Intl. J. Adv. Res. Ideas Innovations Technol., 4: 135-141.