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Capacitance-Toggle Rate Weighting to Optimize Switching Power at Placement Stage of VLSI Conception

[1]Mohammed Darmi, [1]Lekbir Cherif, [1]Jalal Benallal, [2]Rachid Elgouri and [1]Nabil Hmina
[1]Laboratory of Systems Engineering,
[2]Laboratory of Electrical Engineering and Telecommunication Systems,
National School of Applied Sciences, Ibn Tofail University, 14000 Kenitra, Morocco

Abstract: Power consumption is one of the major criteria of an Integrated Circuit (IC) and becomes more important than performance and surface in some applications. Therefore, it is necessary to find new techniques to reduce the power consumed by an IC. This study presents two power-aware techniques: Toggle rate and capacitance-toggle rate weighting which aims to reduce the switching power of nets at the placement stage. These techniques drive the placement engine to reduce the wire length of critical power nets by placing their relative cells close to each other. For an optimal solution, the weighting is applied only on power critical nets that consume more than 80% of the total power in the connection. Experimental results on nine IC industrial designs show an average improvement of 11.8% in total net power and 3.7% of total consumed power.

Key words: Low power, physical design, placement, power optimization, dynamic power, switching activity, performance

INTRODUCTION

For nearly half a century, the evolution of nanotechnologies described by the famous law of Moore allowed improvements to the performances and functionalities of Integrated Circuits (IC) by reducing the geometry of the design, providing a high level of integration and leading to an increase in functional complexity. The ever-increasing complexity of IC has made their power consumption an issue in their own right. It is necessary to take charge of them as early as the architecture phase in the circuit conception and to implement all the adapted techniques to gain control.

There are multiple effects in the Power Optimization (PO) such as an increase in device density, a rising clock frequency, an increasing battery life (i.e., users prefer products that have greater autonomy) and a reduced packaging cost. The higher amount of consumed energy involves greater dissipated heat which also requires a more efficient cooling system.

To control the power consumption, it is necessary to act at each level of the design hierarchy. Every gained microwatt is important. More power is the overall aim of most modern System-on-Chips (SoCs), so, designers tend to search for new methods to lower the design power. To understand the power flow, it is important to start by assimilating the power analysis and some of the optimization methods that occur during all three major design steps: Transaction Modeling Level (TLM), Register Transfer Level (RTL) and physical design implementation.

Rising interest in a power-aware system design has coincided with the adoption of hardware description language SystemC for functional modeling and simulation. By Dhanwada *et al*. (2014), TLM simulation data enables the designer to produce dynamic and leakage power calculations. This development is based on gate level modeling semantics and flows.

As for RTL, power-aware techniques aim to improve the RTL code for low power design. Khalifa and Salah (2016) developed the coded technique that defines the specific input of signals targeted and displays the error signal which may consume extra wasted power. Wang and Roy (2003) split RTL Power Optimization (PO) into two phases: RTL exploration which estimates the power area and delay to adapt the RTL code and gate-level commitment in which accurate power and delay are available to decide whether to keep the changes assigned to the code to optimize the power delay trade-offs.

Low power RTL synthesis (Keating *et al*. 2011), performs a dynamic and static RTL power analysis optimization by inserting the VCD file or switching activity information, adding clock gating to reduce the dynamic power, detecting hot spots and reporting power.

Corresponding Author: Mohammed Darmi, Laboratory of Systems Engineering, National School of Applied Sciences, Ibn Tofail University, 14000 Kenitra, Morocco

In this study, PO that occurs during TLM, RTL and RTL synthesis are the inputs. The interest goes to the last and critical stage before manufacturing the IC which is the physical design implementation called Place and Route (P&R).

In the PO flow happens during the three major steps of the physical design. The placement stage uses power-driven global placement and register clumping. The clock tree synthesis stage is an aggressive multi-bit register swap. Finally, the route stage cleverly utilizes less capacitive metals for high-activity nets for PO.

The objective of this research is to reduce 10% of the switching power of signal nets at the placement stage in the physical design flow without changing the netlist or supply voltages in any way. This study introduces an algorithm that optimizes the switching power by reducing net capacitance.

Literature review

Power consumption in VLSI design: To take consumption into account during the overall design of Systems on Chip (SoC), it is necessary to study the various models developed and to analyze their suitability in relation to an optimization objective at the architecture and system levels. From this analysis, we can determine which models are usable and which we will have to extend or develop.

The consumption of an IC at the transistor level can be broken down into two terms: "static consumption" due mainly to parasitic currents and "dynamic consumption" resulting from the switching activity of circuits (Rabaey *et al.*, 2003).

Our previous study on power consumption of electronic systems hardware in CMOS technology leads us to the expression:

$$P_{total} = P_{dyn} + P_{leak} \tag{1}$$

The dynamic power consumption P_{dyn} occurs during the switching of transistors and depends mostly on the clock frequency, consisting of switching power and internal power.

The static power consumption P_{leak} is the transistor leakage current that flows whenever power is applied to the device independent of the clock frequency or switching activity. Previous research Cousin *et al.* (2000), Macii (1997) report that consumption due to static power represents on average, only a few nano-Amperes (nA:10^{-9}) of the overall consumption of a circuit.

Furthermore, it is mentioned that the short circuit power represents 20-30% of the dynamic consumption and that the switching power represents 70-80% of the overall consumption of a circuit under good conditions. For cells, power model:

$$P_{dyn} = P_{int} + P_{switch} \tag{2}$$

$$P_{int} = \frac{1}{2}(E_{rise} + E_{fall})TR \tag{3}$$

Where:

E_{rise} = Rise Energy
E_{fall} = Fall Energy
TR = Toggle Rate; the number of toggles per time-unit

$$P_{switch} = \frac{1}{2}CV^2TR \tag{4}$$

Where:

C = Total wire Capacitance
V = Power supply Voltage

For nets, the power model is:

$$P_{dyn} = \frac{1}{2}CV^2TR \tag{5}$$

The main goal of this research is to present a new method that helps to reduce the net's capacitance on a list of critical nets by weighting their TR.

MATERIALS AND METHODS

Placement power aware algorithms

Placement algorithms: The placement involves assigning the standard cells of the circuit. Almost every place and route tool uses a two-step approach (global and detail placement) to place standard cell instances.

Moreover, several placement techniques have been described in the literature: "Mincut" placement (Breuer, 1977), based on utilizing partitioning to perform placement; terminal propagation (Dunlop and Kernighan, 1985), based on quadratic placement; Gordian placement (Kleinhans *et al.*, 1991) and the "Timber Wolf" algorithm (Sun and Sechen, 1995) based on simulated annealing (Reyes and Steidley, 1998).

These research aimed to optimize The Wirelengths (TWL) used for routing the circuit by making some targeted nets shorter during placement which may sacrifice the wirelengths of other nets that are connected through common cells. This consists of several iterations to find the best placement of the standard cell based on a cost function that includes the constraints of placement.

The placement objective is to determine the locations and orientations of all circuit's elements within a layout, given solution constraints (no overlapping cells) and optimization goals (minimizing timing and total wire length). Since, the delay of a net directly correlates with the net's length, placers often minimize total wire length.

Placement power-aware algorithms: According to Eq. 3-5 to minimize the wire-length, we used two important factors: TR, the rate at which net switches compared to its input (s) and C, the net capacity factor.

To optimize the nets using the net weighting technique, two algorithms were developed: Toggle Rate weighting (TR weighting), to select and weight the nets with a higher switching activity and Capacitance-Toggle Rate weighting (C-TR weighting), to select and weight the nets with a higher product C*TR.

Algorithm 1; TR weighting:

```
Input
    Database before placement
    Enable power scenario
Output:
    New_weight.db
Algorithm:
Get the Percentage (P%) of nets to weight
Calculate N = Number of P nets
Set list S of the nets switching activity, the property of which is an output and not a clock
Sort list S decreasingly
Set S1 with rang = N
Set switching = last element of the list S1
For each net N in the list S
If TR (N) ≥ switching the New_Weight (N) = fac * switching_activity (N)
```

In a stage in which the chip is unplaced, Algorithm 1 yields the percentage of the nets to be weighted and assigns the weights to their switching rates. Thus, the nets with a higher TR after the placement will have a shorter wire length and vice versa.

The results of the first algorithm show an increased wire length in some signal nets with a lower switching activity. However, these nets don't really affect the power consumption because TR≅0.

Additionally, assigning a large weight to the signal net with higher switching rate is useless because the TRs of all nets stay the same during the placement stage. Therefore, the second algorithm was added to include the capacitance as a dynamic parameter to the cost function of the weighting process.

Algorithm 2; C-TR weighting:

```
Input
    Database after first placement
    Enable power scenario
Output:
    New_weight.db
Algorithm:
Set P% percent of nets
Calculate N = number of P net
Set list L of nets with higher consumed energy and with a range equal to N
For each net N in the list L
New_Weight = Capacitance * switching_activity (N) + default_Weight
```

For the full "Place and Route" (P&R) of all test-case designs, the EDA tool Nitro-SoC™ (Mentor Graphics PnR tool: was used with a low-power capability that enables dynamic and leakage power optimization throughout the power-aware flow.

To have a complete picture of the optimization technique, four types of P&R flow were used: default full flow with no power reduction (NONE); power-driven flow with cell optimization (LOW POWER); NONE+Algorithms and LOW POWER+Algorithms. Detailed analysis was done on a specific net with a high toggle rate.

RESULTS AND DISCUSSION

Table 1 shows the design characteristics of all test-cases used to validate the optimization methods. This allows a clear vision of the power improvement on the real designs. Figure 1 shows a wire length reduction after applying Algorithm 2 from 1182-717 μm. Because of the wire length reduction, wire capacitance and dynamic power were also reduced. Figure 2 shows the significant net capacitance and power reduction (Fig. 2b) compared to the baseline (Fig. 2a).

The optimization technique highlighted a list of nets with high toggle rates in the Nitor-SoC Graphical User Interface (GUI). In Fig. 3, a good clustering of nets in a smaller area compared to the default case was detected. The total dynamic power of all selected nets was reduced from 0.7-0.4 mW.

Table 2 summarizes the results of the "Low Power" flow compared to the "low power+algorithm 2" flow at the end of the placement stage for the nine industrial designs tested. For each design, the timing and percentage improvements in terms of cells, nets, total power and global wire-length are shown for the baseline and the tested flows.

Table 1: List of designs for validation

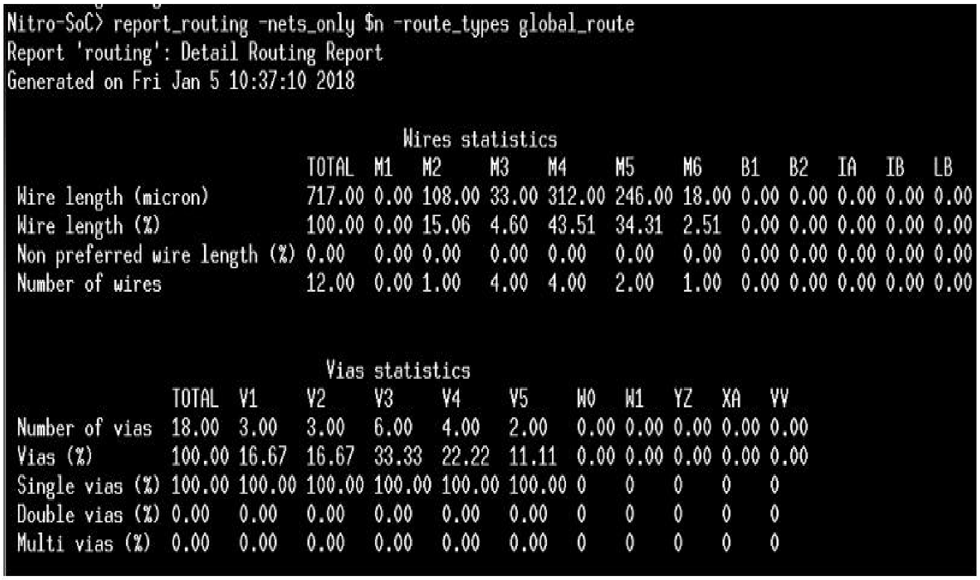
Designs	Technology (nm)	Cells count (million)	Area (mm^2)
1	28	0.13	0.14
2	28	0.64	1.80
3	28	4.96	6.32
4	28	2.74	4.59
5	28	2.31	3.08
6	28	3.85	6.19
7	28	2.20	2.90
8	16	0.64	0.40
9	16	0.82	0.49

Table 2: Results of the "LOW POWER" Flow compared to "LOW POWER+Algorithm 2" flow

Designs gain = % (proposed flow-baseline)/baseline/Variables	Timing (nsec)	Cells power (mW)	Nets power (mW)	Total power (mW)	Wire-length (m)
1					
Baseline: LOW POWER	-2.206	2472.268	2644.487	5116.755	1.48
LOW POWER+Algorithm 2	-3.651	2617.921	2336.493	4954.414	1.48
Gain		5.89%	-11.65%	**-3.17%**	
2					
Baseline: LOW POWER	-0.001	300.807	324.478	625.285	0.21
LOW POWER+Algorithm 2	-0.007	303.093	306.085	609.178	0.23
Gain		0.76%	-5.67%	**-2.58%**	
3					
Baseline: LOW POWER	-1.318	1731.212	2071.505	3802.717	1.41
LOW POWER+Algorithm 2	-4.422	1845.773	1936.408	3782.181	1.54
Gain		6.62%	-6.52%	**-0.54%**	
4					
Baseline: LOW POWER	-0.062	598.468	485.824	1084.292	0.66
LOW POWER+Algorithm 2	-1.073	580.279	416.611	996.889	0.68
Gain		-3.04%	-14.25%	**-8.06%**	
5					
Baseline: LOW POWER	-0.657	1065.521	984.158	2049.678	0.58
LOW POWER+Algorithm 2	-1.107	1084.589	892.81	1977.400	0.62
Gain	68.49%	1.79%	-9.28%	**-3.53%**	
6					
Baseline: LOW POWER	-0.002	36.712	35.105	71.818	0.87
LOW POWER+Algorithm 2	-0.004	36.715	30.857	67.572	0.89
Gain		0.01%	-12.10%	**-5.91%**	
7					
Baseline: LOW POWER	0.067	1435.84	1614.34	3050.67	59.01
LOW POWER+Algorithm 2	0.085	1531.95	1412.76	2944.61	57.18
Gain		6.69%	-12.49%	**-3.48%**	
8					
Baseline: LOW POWER	-2.183	189.286	73.177	262.40	0.93
LOW POWER + Algorithm 2	-1.449	201.457	61.342	262.40	0.99
Gain		6.43%	-16.17%	**0.00%**	
9					
Baseline: LOW POWER	-16.239	249.629	78.451	328.08	0.12
LOW POWER + Algorithm 2	-15.436	243.839	64.372	308.21	0.13
Gain		-2.32%	-17.95%	**-6.06%**	

Bold values are significant

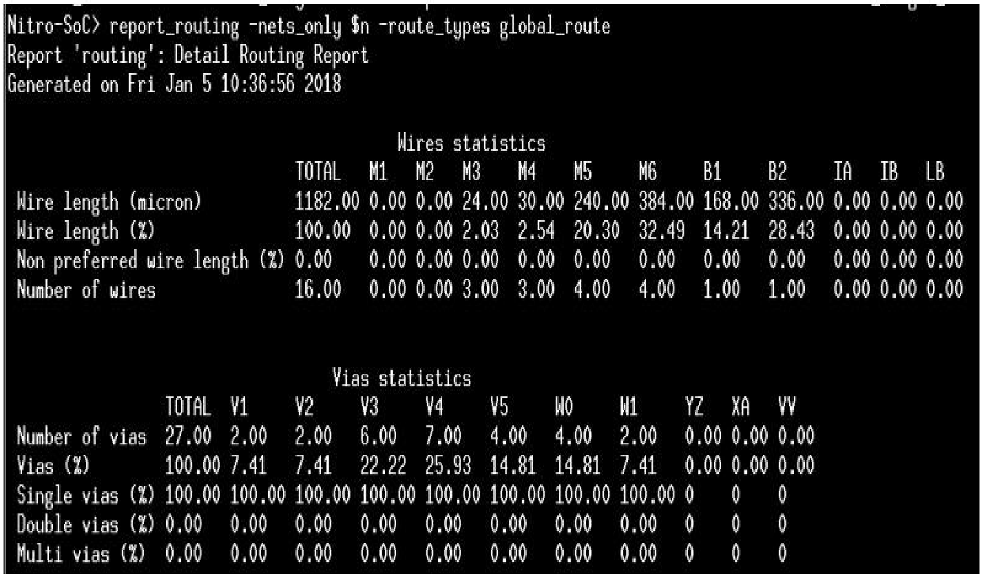
(a)



```
Nitro-SoC> report_routing -nets_only $n -route_types global_route
Report 'routing': Detail Routing Report
Generated on Fri Jan 5 10:37:10 2018

                                    Wires statistics
                              TOTAL  M1   M2     M3    M4     M5     M6    B1   B2   IA   IB   LB
 Wire length (micron)         717.00 0.00 108.00 33.00 312.00 246.00 18.00 0.00 0.00 0.00 0.00 0.00
 Wire length (%)              100.00 0.00 15.06  4.60  43.51  34.31  2.51  0.00 0.00 0.00 0.00 0.00
 Non preferred wire length (%) 0.00  0.00 0.00   0.00  0.00   0.00   0.00  0.00 0.00 0.00 0.00 0.00
 Number of wires              12.00  0.00 1.00   4.00  4.00   2.00   1.00  0.00 0.00 0.00 0.00 0.00


                               Vias statistics
                 TOTAL  V1     V2     V3     V4     V5     W0   W1   YZ   XA   VV
 Number of vias  18.00  3.00   3.00   6.00   4.00   2.00   0.00 0.00 0.00 0.00 0.00
 Vias (%)        100.00 16.67  16.67  33.33  22.22  11.11  0.00 0.00 0.00 0.00 0.00
 Single vias (%) 100.00 100.00 100.00 100.00 100.00 100.00 0    0    0    0    0
 Double vias (%) 0.00   0.00   0.00   0.00   0.00   0.00   0    0    0    0    0
 Multi vias (%)  0.00   0.00   0.00   0.00   0.00   0.00   0    0    0    0    0
```

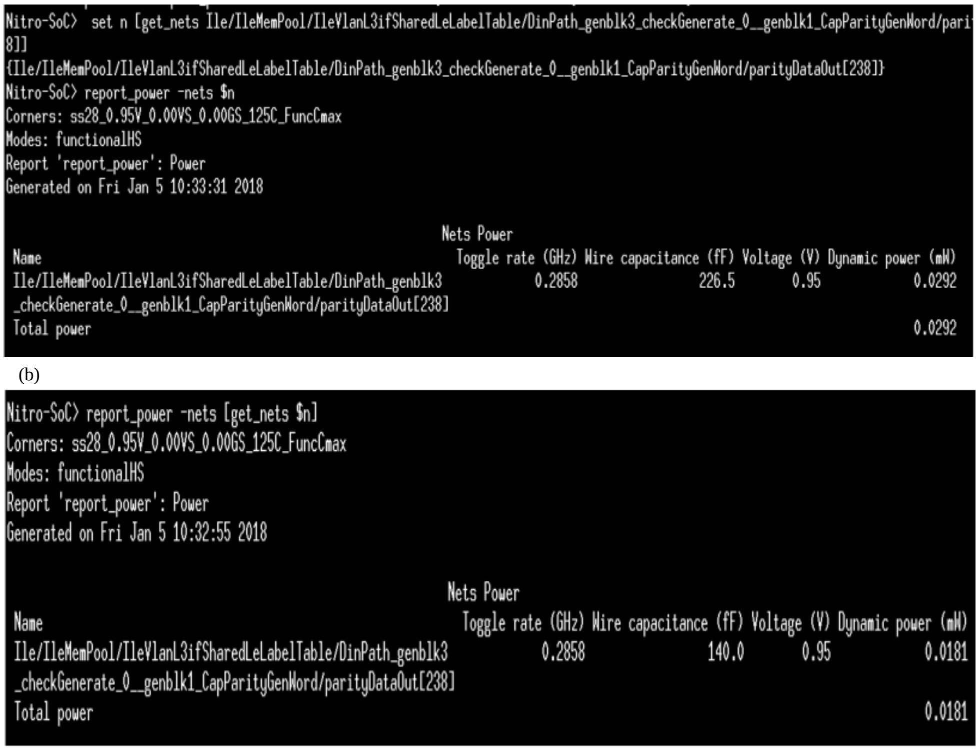
Fig. 1: Continue

(b)



```
Nitro-SoC> report_routing -nets_only $n -route_types global_route
Report 'routing': Detail Routing Report
Generated on Fri Jan 5 10:36:56 2018

                                          Wires statistics
                             TOTAL   M1   M2   M3    M4    M5     M6     B1     B2     IA   IB   LB
 Wire length (micron)        1182.00 0.00 0.00 24.00 30.00 240.00 384.00 168.00 336.00 0.00 0.00 0.00
 Wire length (%)             100.00  0.00 0.00 2.03  2.54  20.30  32.49  14.21  28.43  0.00 0.00 0.00
 Non preferred wire length (%) 0.00  0.00 0.00 0.00  0.00  0.00   0.00   0.00   0.00   0.00 0.00 0.00
 Number of wires             16.00   0.00 0.00 3.00  3.00  4.00   4.00   1.00   1.00   0.00 0.00 0.00


                                    Vias statistics
                 TOTAL  V1     V2     V3     V4     V5     W0     W1     YZ   XA   YY
 Number of vias  27.00  2.00   2.00   6.00   7.00   4.00   4.00   2.00   0.00 0.00 0.00
 Vias (%)        100.00 7.41   7.41   22.22  25.93  14.81  14.81  7.41   0.00 0.00 0.00
 Single vias (%) 100.00 100.00 100.00 100.00 100.00 100.00 100.00 100.00 0    0    0
 Double vias (%) 0.00   0.00   0.00   0.00   0.00   0.00   0.00   0.00   0    0    0
 Multi vias (%)  0.00   0.00   0.00   0.00   0.00   0.00   0.00   0.00   0    0    0
```

Fig. 1: Net wire length report: a) Baseline and b) Proposed flow



(a)

```
Nitro-SoC>  set n [get_nets Ile/IleMemPool/IleVlanL3ifSharedLeLabelTable/DinPath_genblk3_checkGenerate_0__genblk1_CapParityGenWord/pari
8]]
{Ile/IleMemPool/IleVlanL3ifSharedLeLabelTable/DinPath_genblk3_checkGenerate_0__genblk1_CapParityGenWord/parityDataOut[238]}
Nitro-SoC> report_power -nets $n
Corners: ss28_0.95V_0.00VS_0.00GS_125C_FuncCmax
Modes: functionalHS
Report 'report_power': Power
Generated on Fri Jan 5 10:33:31 2018

                                                   Nets Power
 Name                                                Toggle rate (GHz) Wire capacitance (fF) Voltage (V) Dynamic power (mW)
 Ile/IleMemPool/IleVlanL3ifSharedLeLabelTable/DinPath_genblk3    0.2858                226.5       0.95              0.0292
 _checkGenerate_0__genblk1_CapParityGenWord/parityDataOut[238]
 Total power                                                                                                         0.0292
```

(b)

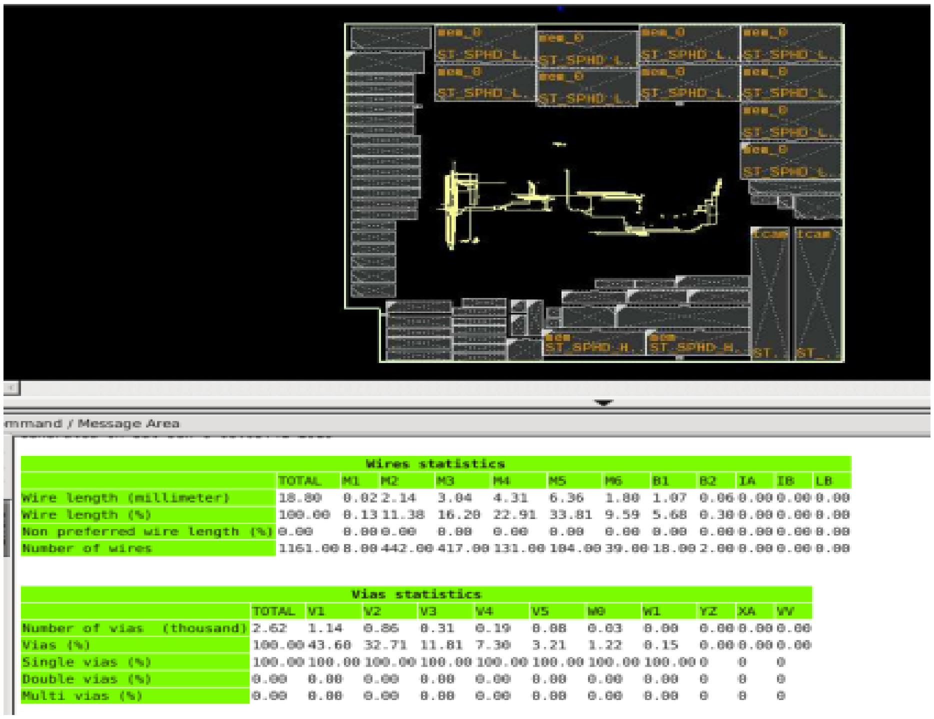
```
Nitro-SoC> report_power -nets [get_nets $n]
Corners: ss28_0.95V_0.00VS_0.00GS_125C_FuncCmax
Modes: functionalHS
Report 'report_power': Power
Generated on Fri Jan 5 10:32:55 2018

                                                   Nets Power
 Name                                                Toggle rate (GHz) Wire capacitance (fF) Voltage (V) Dynamic power (mW)
 Ile/IleMemPool/IleVlanL3ifSharedLeLabelTable/DinPath_genblk3    0.2858                140.0       0.95              0.0181
 _checkGenerate_0__genblk1_CapParityGenWord/parityDataOut[238]
 Total power                                                                                                         0.0181
```

Fig. 2: Net capacitance and power report: a) Baseline and b) Proposed flow

According to Table 2, the low power with weighting flow achieves an average improvement of 11.79% (ranging from 5.67-17.95%) in all nets power and an average improvement of 3.70% (ranging from 0-8.06%) in total power. Global route wire-length has slightly increased due to more timing optimization after power-aware placement.

In general, for the timing, the degradation is minor compared to the important power gain and could be ignored. In some cases, the power consumed by the cells increases due to the need to optimize the timing after favoring the nets with a high toggle rate. Overall, the total power is well optimized because of the

(a)



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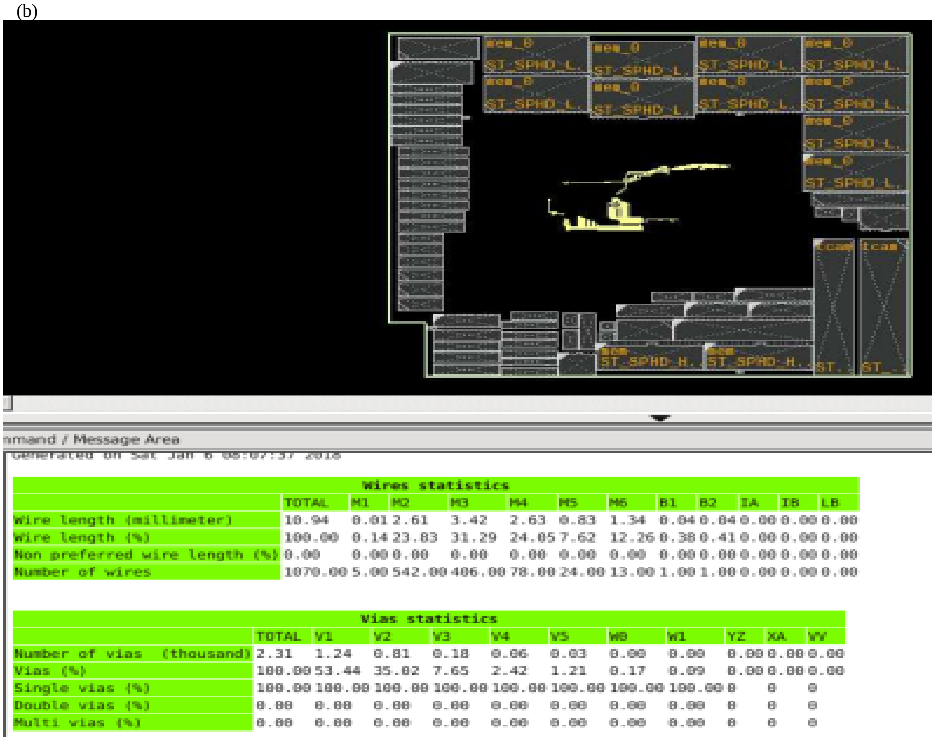
Wires statistics												
	TOTAL	M1	M2	M3	M4	M5	M6	B1	B2	IA	IB	LB
Wire length (millimeter)	18.80	0.02	2.14	3.04	4.31	6.36	1.80	1.07	0.06	0.00	0.00	0.00
Wire length (%)	100.00	0.13	11.38	16.20	22.91	33.81	9.59	5.68	0.30	0.00	0.00	0.00
Non preferred wire length (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Number of wires	1161.00	8.00	442.00	417.00	131.00	104.00	39.00	18.00	2.00	0.00	0.00	0.00

Vias statistics											
	TOTAL	V1	V2	V3	V4	V5	W0	W1	YZ	XA	VV
Number of vias (thousand)	2.62	1.14	0.86	0.31	0.19	0.08	0.03	0.00	0.00	0.00	0.00
Vias (%)	100.00	43.60	32.71	11.81	7.30	3.21	1.22	0.15	0.00	0.00	0.00
Single vias (%)	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	0	0	0
Double vias (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0	0	0
Multi vias (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0	0	0

(b)



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Wires statistics												
	TOTAL	M1	M2	M3	M4	M5	M6	B1	B2	IA	IB	LB
Wire length (millimeter)	10.94	0.01	2.61	3.42	2.63	0.83	1.34	0.04	0.04	0.00	0.00	0.00
Wire length (%)	100.00	0.14	23.83	31.29	24.05	7.62	12.26	0.38	0.41	0.00	0.00	0.00
Non preferred wire length (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Number of wires	1070.00	5.00	542.00	406.00	78.00	24.00	13.00	1.00	1.00	0.00	0.00	0.00

Vias statistics											
	TOTAL	V1	V2	V3	V4	V5	W0	W1	YZ	XA	VV
Number of vias (thousand)	2.31	1.24	0.81	0.18	0.06	0.03	0.00	0.00	0.00	0.00	0.00
Vias (%)	100.00	53.44	35.02	7.65	2.42	1.21	0.17	0.09	0.00	0.00	0.00
Single vias (%)	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	0	0	0
Double vias (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0	0	0
Multi vias (%)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0	0	0

Fig. 3: Nets wire highlighting in the GUI: a) Baseline and b) Proposed flow

significant power reduction on the nets. In all the tested cases, only one design gets an improvement of 0%. This remains a good result as long as the same Quality of Result (QoR) at the end was obtained.

CONCLUSION

This research proposed a "placement power aware" solution for the reduction of interconnected power in the placement stage. The proposed algorithm proved its worth on several designs made with 28 and 16 nm technology nodes. A gain of 3.70% in total power consumption was achieved. The compliance of the results suggests a promising future for VLSI design because even if the manufacturer of the integrated circuit continues reducing device features, low power and high performance could be reached.

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