

The Effect of Using Filter on Total Harmonic Distortion in Multilevel Inverter

¹Jameel Kadhum Abed, ²Mohannad Jabbar Mnati and ¹Bassam Mohammed Yaseen

^{1,3}Electrical Engineering Technical College, Middle Technical University, Al-Dora Baghdad, Iraq

²Department of Electrical Energy, Metals, Mechanical Constructions and Systems, Ghent University, Technologiepark Zwijnaarde 913, B-9052 Zwijnaarde, Gent, Belgium

Abstract: Multi-level inverter used in applications that require high power. The important factor in multi-level inverter is Total Harmonic Distortion (THD). This study discuss nine level cascaded H-bridge multilevel inverter. Also, proposed the effects of using filter on waveform and Total Harmonic Distortion (THD) of output voltage and current. Discussed LC low pass filter and sinusoidal pulse width modulation as control technique of switches. Comparison THD of nine level cascaded H-bridge multilevel inverter with and without filter. The proposed level and filter are design and simulate by MATLAB 2010 Version 7.11.0. The simulation results show the effects of using filter on THD and waveform of output voltage and current. Different methods for choosing filter value are used to illustrate the filter effect.

Key words: Cascaded H-Bridge Multilevel Inverter (CHBMLI), Sinusoidal Pulse Width Modulation (SPWM), Low Pass Filter (LPF), design, output voltage, current

INTRODUCTION

Multilevel Inverter (MLI) is a device uses series of semiconductor switches to convert DC power into AC power with stepped wave. The presence of applications that need high power increases the demand of using multi-level inverter instead of conventional inverter (Two level inverter) (Krishna and Deepthi, 2014; Sangolkar and Salodkar, 2014). MLI has some advantages over conventional inverter are: lower THD, higher output power and smaller output filter (Sudarsanan *et al.*, 2015).

Multilevel inverter used in many applications such as variable speed drive, Flexible AC Transmission Systems (FACTS) and renewable energy such as wind, full cells and photovoltaic (Peng, 2001; Shojaei *et al.*, 2010). There are three different topologies of multi-level inverter are: Flying Capacitance Multilevel Inverter (FCMLI), Diode Clamped Multilevel Inverter (DCMLI) and Cascaded H-Bridge Multilevel Inverter (CHBMLI) (Chaturvedi *et al.*, 2014; Azli and Choong, 2006; Priyan and Ramani, 2013).

Cascaded H-bridge inverter is preferred because of simplest design and less cost as compared with the other two types. The problem of MLI is high THD at early levels. To reduce the THD of output Voltage (V_o) at the

same level used the best method of control methods and sometimes used the filter (Ahmad and Khan, 2012). The filter decreases the THD and improving the waveform of output voltage and current also the performance and efficiency of multilevel inverter are improve (Kim *et al.*, 2000).

The research paper obtained on nine level cascaded H-bridge multi-level inverter with and without filter. Different methods of choosing filter value are proposed to show the effect of using filter on waveforms and THD of output voltage and current. LC Low Pass Filter (LPF) are discussed also Sinusoidal Pulse Width Modulation (SPWM) is proposed and used as a control method.

MATERIALS AND METHODS

Cascaded H-Bridge Inverter (CHBMLI): H-bridge inverter (Full bridge inverter) consists of four semiconductor switches (S_1 - S_4) and one DC source. Figure 1 shows single H-bridge inverter. Single H-bridge inverter generates three different steps of voltages: $+V_{DC}$, 0 and $-V_{DC}$ (Malinowaski *et al.*, 2010). When S_1 and S_4 are turn on the voltage at output terminals is $+V_{DC}$, when S_2 and S_3 are turn on the voltage at output terminals is $-V_{DC}$ and when S_1 - S_4 are turn

on there is no voltage on output terminals ($V_o = 0$) but the current passes. Each H-bridge need two sets of pulses to control: upper pulses and lower pulses. The group of H-bridge inverter connects in series to configure cascaded H-bridge inverter (Malinowaski *et al.*,

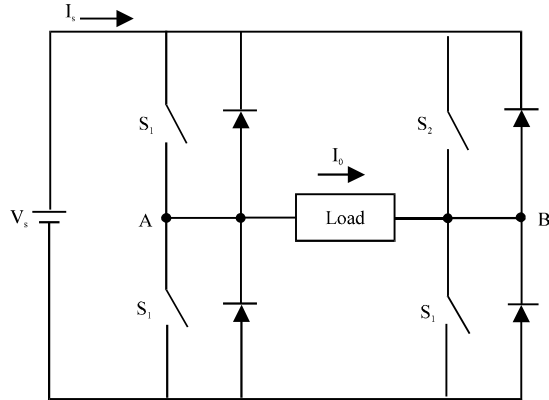


Fig. 1: Single H-bridge inverter (Malinowaski *et al.*, 2010)

2010). The advantages of CHBMLI are needs the least number of components and low switching frequency (Booma and Sridhar, 2011) while the disadvantage is needs multiple DC sources. The total voltage of CHBMLI is the sum of all voltages generated from each H-bridge inverter.

Single phase 9 level CHBMLI: Nine level CHBMLI consists of five full bridge, five DC sources and five balance capacitances. The steps voltage of this level are: $+4V_{DC}$, $+3V_{DC}$, $+2V_{DC}$, $+V_{DC}$, 0 , $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$ and $-4V_{DC}$. Figure 2a shows the circuit diagram of 9 level CHBMLI and Fig. 2b shows the output voltage waveform of nine level CHBMLI. The switches status of each level of output voltage shown in Table 1.

Sinusoidal PWM techniques (SPWM): SPWM is a common method for generating pulses to semiconductor switches. SPWM used to reduce the distortion of MLI. The generation of pulses depends on interfacing of two

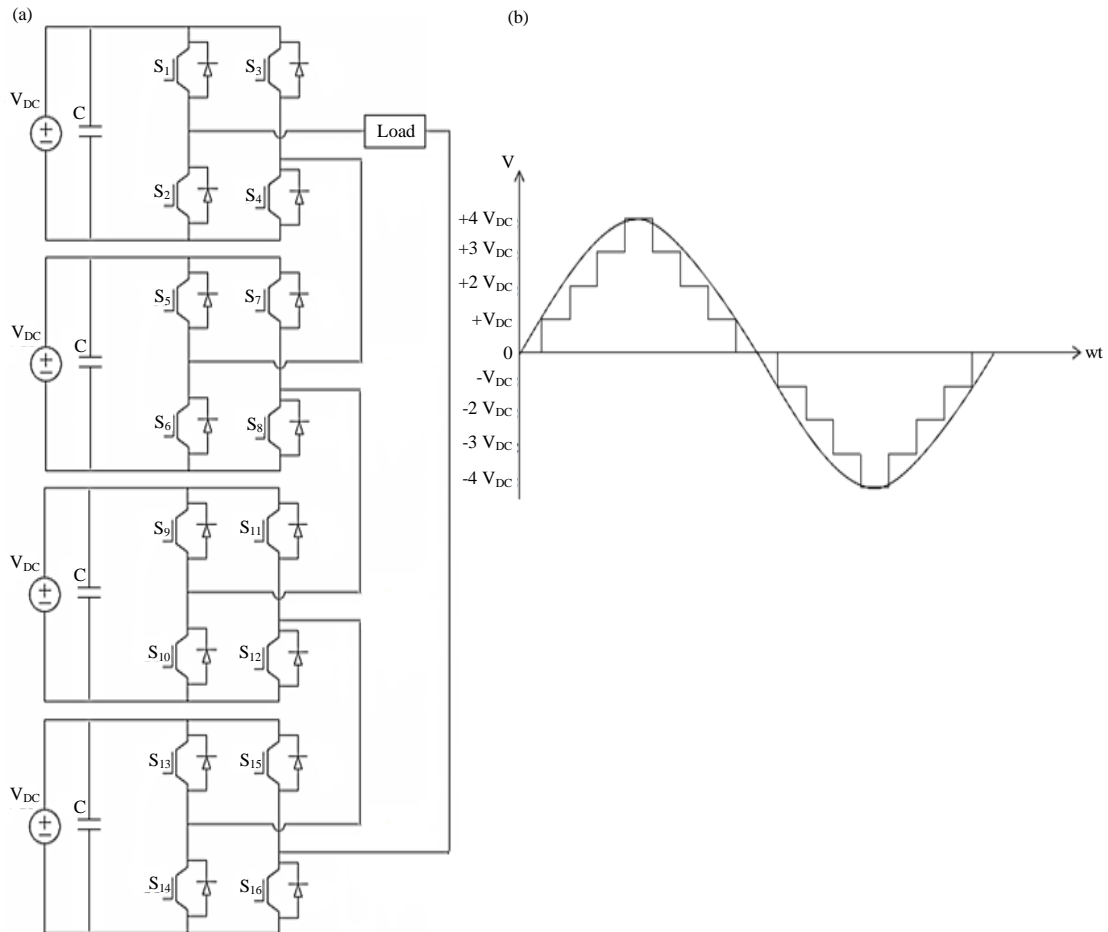


Fig. 2a: Circuit diagram of nine level CHBMLI; b) Output voltage waveform nine level CHBMLI

Table 1: Switches status of nine level of CHBMLI

Output voltage level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
$+V_{DC}$	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1
$+2 V_{DC}$	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1
$+3 V_{DC}$	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1
$+4 V_{DC}$	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$-V_{DC}$	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1
$-2 V_{DC}$	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1
$-3 V_{DC}$	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
$-4 V_{DC}$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

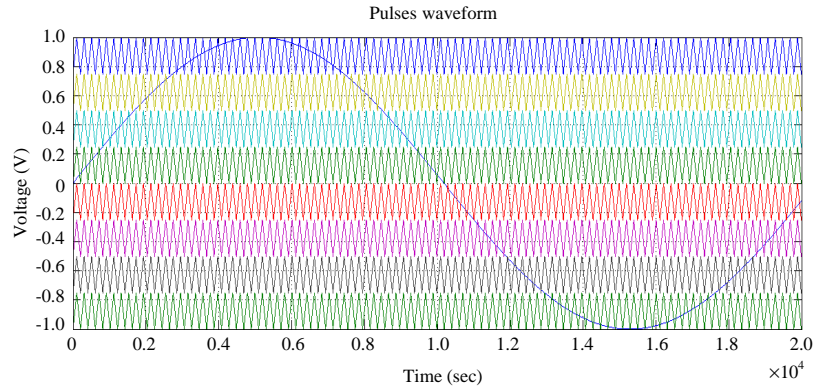


Fig. 3: Switching pulses of nine level CHBMLI

signals: modulating signal and carrier signals. The modulating signal is a singular and sinusoidal wave. The carrier signals are several and triangular waves (Rodriguez *et al.*, 2002).

The carrier signal frequency is higher than modulating signal frequency. The switch is turn on when the amplitude of carrier signal is greater than modulating signal. But when the amplitude of modulating signal is greater than carrier signal the switch is turn off. The numbers of triangular waves are (m-1) where m is the number of level. This method used to decrease the size of filter to minimum (Krishna and Deepthi, 2014). Figure 3 shows the generation of pulses to nine level CHBMLI.

LC Low Pass Filter (LC-LPF): The filter used to decrease the distortion of output voltage waveform and improving the shape of wave and approaching to the sinusoidal wave. The design of filter depends on the effectiveness, cost, size and weight (Dahono and Purwadi, 1995). The ideal filter is not always preferred because it is possible to be expensive as compared to its performance also the weight and size may be not suitable with inverter design. The filter connects in parallel with the output terminals of CHBMLI (Kim *et al.*, 2000). Figure 4 shows the circuit of LC-LPF.

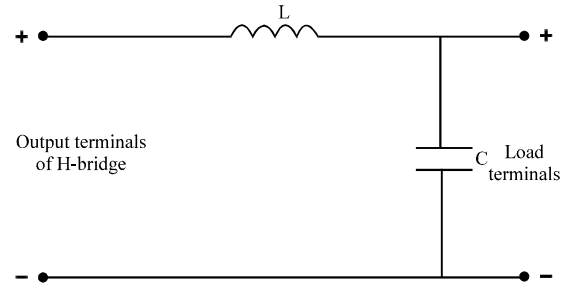


Fig. 4: LC-LPF circuit

RESULTS AND DISCUSSION

Results of MATLAB\Simulink: All results of the proposed CHBMLI level, SPWM and LC-LPF are shown below have been done by MATLAB. Output Voltage (V_o) and output current (I_o) waveforms are showed by scope also voltage THD (THD_v) and current THD (THD_i) are achieved by FFT spectrum of output voltage and current waveforms. The results obtained at RL load ($R = 100 \Omega$ and $L = 0.5 H$).

Case 1; Nine level without filter: V_o waveform, THD_v , I_o waveform and THD_i are shown in Fig. 5-8, respectively. V_o waveform has ripples and THD_v spectrum is 13.63%. I_o waveform has very low distortion and its THD spectrum is 3.04%.

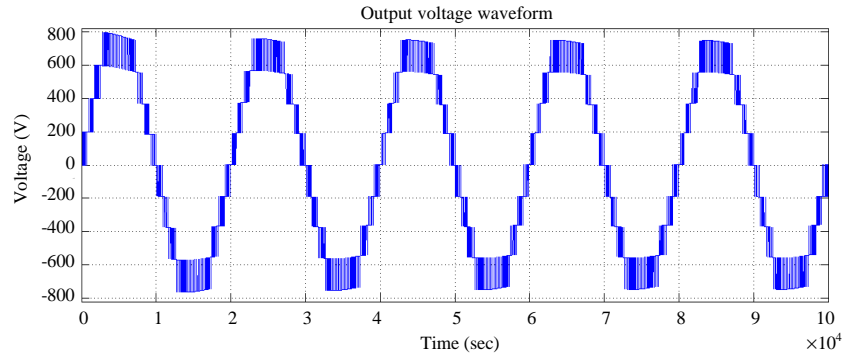


Fig. 5: V_o waveform

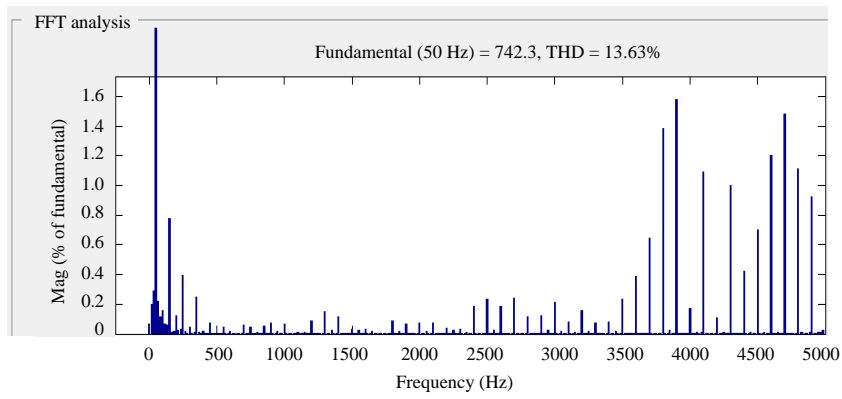


Fig. 6: THD_v

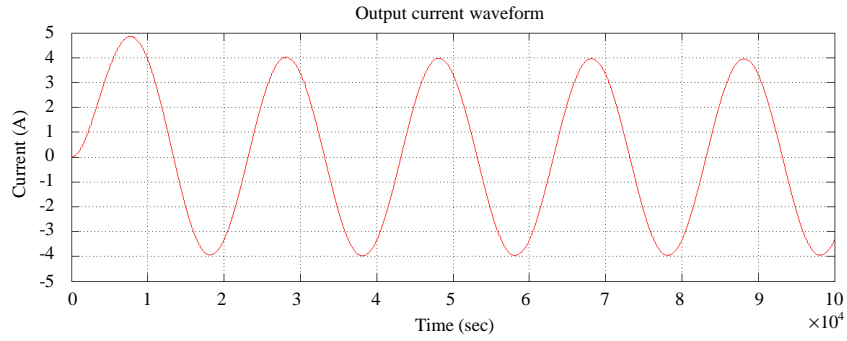


Fig. 7: I_o waveform

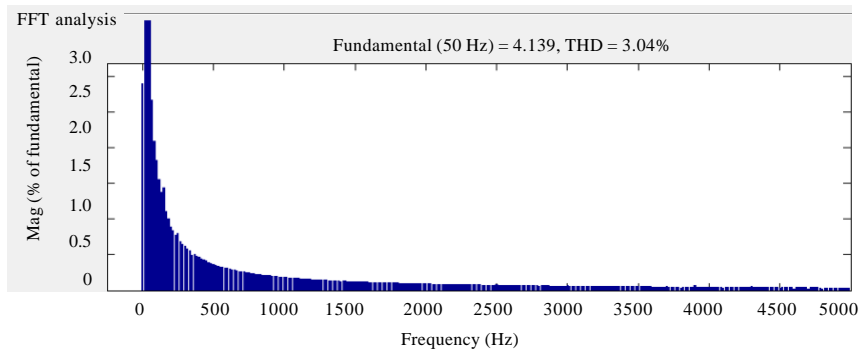


Fig. 8: THD_i

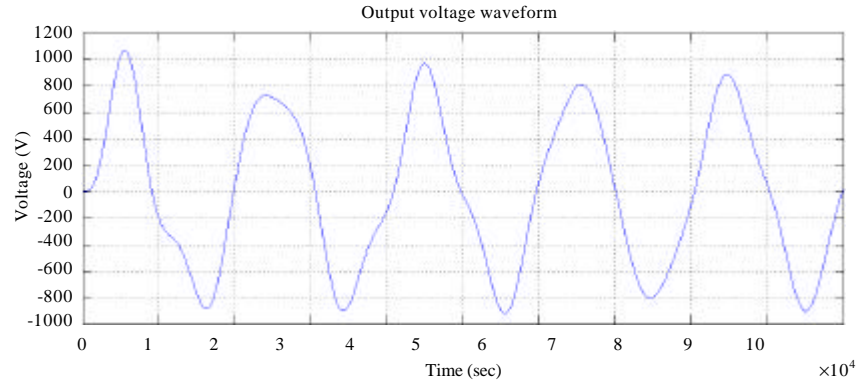


Fig. 9: V_o waveform

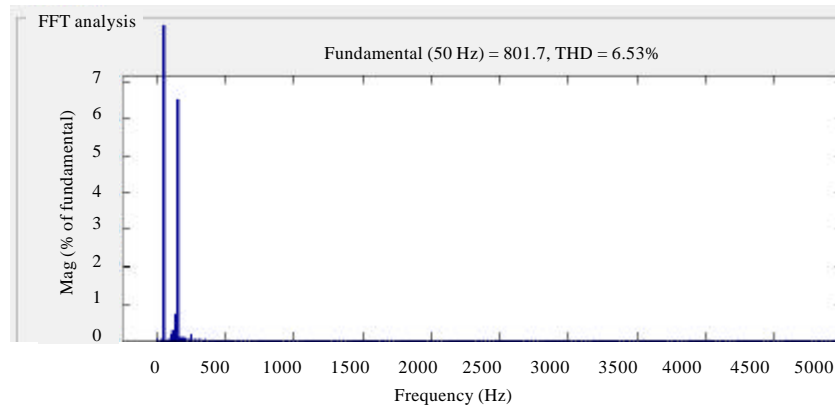


Fig. 10: THD_v

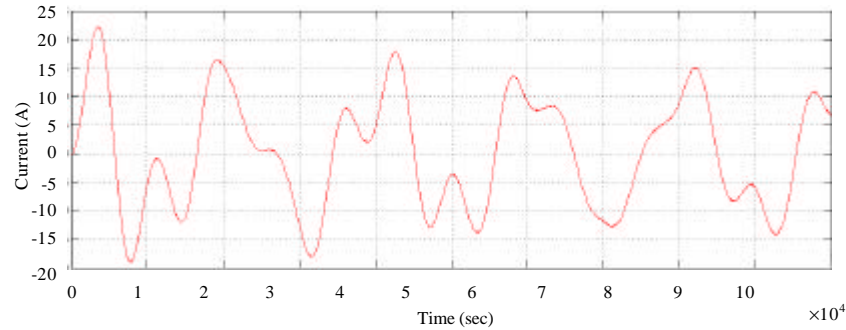


Fig. 11: I_o waveform

Case 2; Nine level with first filter: Some researchers depend on try and error method to choose the value of filter (Chacko and Thomas, 2014). The filter that chosen in this method must be simulate before hardware design to show the effect of this filter value on waveforms and THD of output voltage and current.

If use 2 mH and 10 μ F, then the results of V_o waveform and THD also the current waveform and THD can be show in Fig. 9-12, respectively. The V_o waveform is not uniform also has its THD is 6.53%. waveform of I_o has high distrtrion and THD_i is 24.58%. The filter has bad effect in this case.

Case 3; Nine level with second filter: The filter in this case is chosen according to law $f_c = 1/2\pi\sqrt{LC}$, where f_c is carrier frequency. In unipolar method $f_c = 2f_s$, where f_s is switching frequency. $f_s = 5$ kHz in design. Choose $C = 50$ μ F then $L = 5$ μ H. This vale of filter is used and the simulink results are obtains below.

Figure 13 shows waveform of V_o and its more smooth than preivious cases. Figure 14 shows THD_v is 0.77% and it is very low. I_o waveform is less ripple and shown in Fig. 15. THD_i is 2.69%, this value is the least current distortion as shown in Fig. 16.

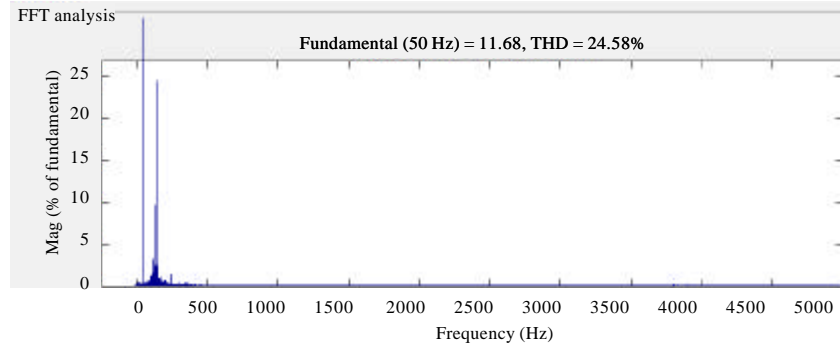


Fig. 12: THD_I

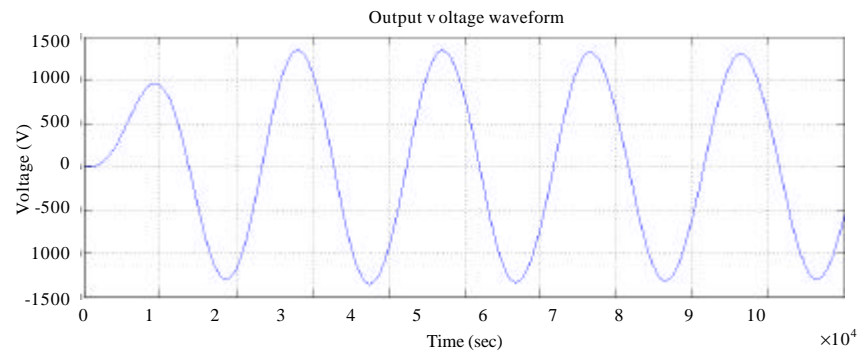


Fig. 13: V_O waveform

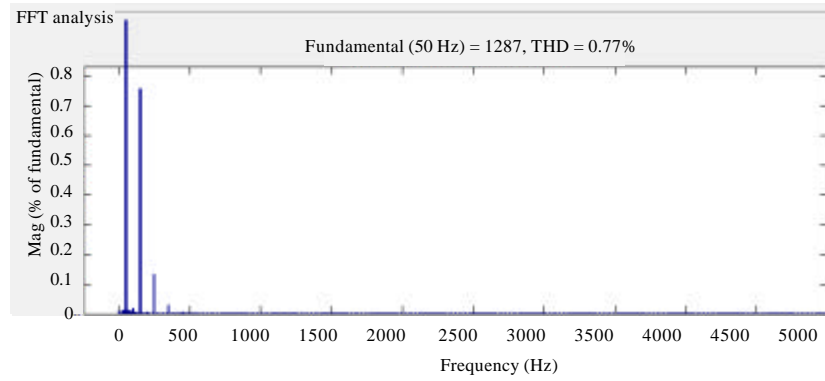


Fig. 14: THD_V

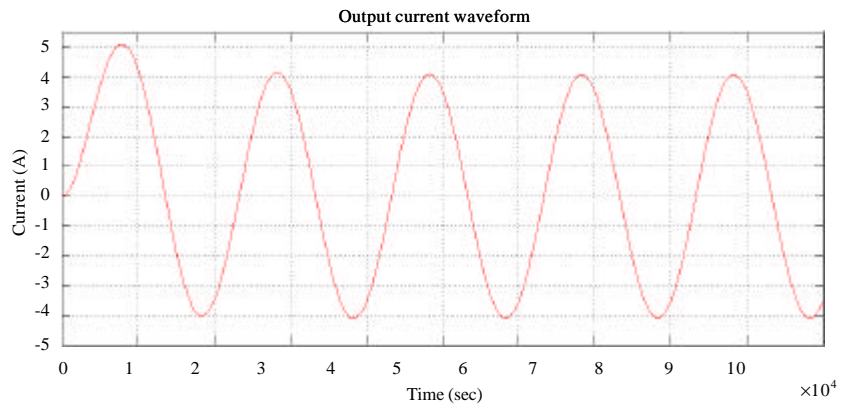


Fig. 15: I_O waveform

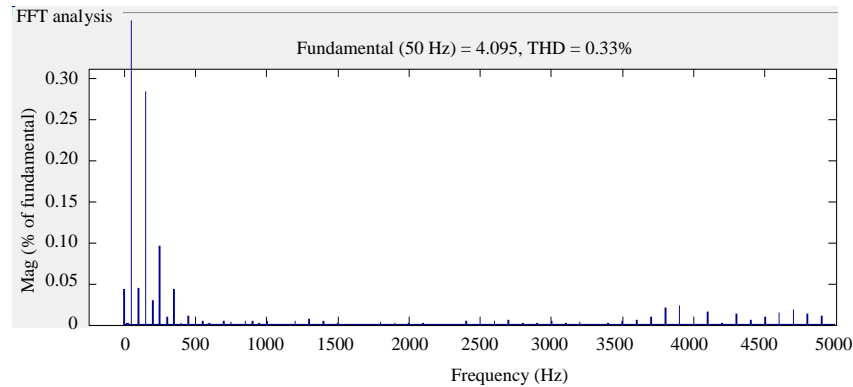


Fig. 16: THD_i

Table 2: Comparison between nine level Inverter with and without filter

Parameters	Without filter	1st filter (L = 2 mH, C = 10 μ F)	2nd filter (L = 5 μ H, C = 50 μ F)
THD _v (%)	13.63	6.53	0.77
THD _i (%)	3.04	24.58	0.33
Cost	Less	Medium	More
Weight	Less	Medium	More

Comparison between nine level inverter/phase with and without using filter: Table 2 shows the comparison between the nine level inverter with and without filter.

CONCLUSION

This study cascaded H-bridge inverter and the effect of using filter on Total Harmonic Distortions (THD), waveforms of output Voltage (V_o) and current (I_o). The result of MATLAB/Simulink shows the THD and waveform of both output voltage and current of nine level CHBMLI. The results of first case are acceptable at some load, only THD_v is slightly high. The values of THDs are good also V_o waveform close to sine wave and output current (I_o) is good. Using first filter improves THD_v and waveform of V_o but the waveform of output current (I_o) become bad and has high ripples. But when using the second filter, THD_v and V_o waveform are more improving also the waveform of output current is improved. The weight, size and cost of second are more than the first filter but the result is more important than size and cost. The choosing of filter depends on the performance and efficiency.

REFERENCES

Ahmad, M. and B.H. Khan, 2012. New approaches for harmonic reduction in solar inverters. Proceedings of the Students Conference on Engineering and Systems, March 16-18, 2012, IEEE, Allahabad, Uttar Pradesh, India, ISBN:978-1-4673-0456-6, pp: 1-6.

Azli, N.A. and Y.C. Choong, 2006. Analysis on the performance of a three-phase cascaded H-bridge multilevel inverter. Proceedings of the IEEE International Conference on Power and Energy (PECon'06), November 28-29, 2006, IEEE, Putra Jaya, Malaysia, ISBN:1-4244-0273-5, pp: 405-410.

Booma, N. and N. Sridhar, 2011. Nine level cascaded H-bridge multilevel DC-link inverter. Proceedings of the International Conference on Emerging Trends in Electrical and Computer Technology (ICETECT), March 23-24, 2011, IEEE, Nagercoil, India, ISBN:978-1-4244-7923-8, pp: 315-320.

Chacko, S. and J. Thomas, 2014. THD analysis of multilevel inverter with different loads. Intl. J. Adv. Res. Electr. Electron. Instrum. Eng., 3: 200-204.

Chaturvedi, P., S. Jain and P. Agarwal, 2014. Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter. IEEE Trans. Ind. Electron., 61: 613-624.

Dahono, P.A. and A. Purwadi, 1995. An LC filter design method for single-phase PWM inverters. Proceedings of the International Conference on Power Electronics and Drive Systems, February 21-24, 1995, IEEE, Singapore, ISBN:0-7803-2423-4, pp: 571-576.

Kim, J., J. Choi and H. Hong, 2000. Output LC filter design of voltage source inverter considering the performance of controller. Proceedings of the International Conference on Power System Technology (PowerCon 2000) Vol. 3, December 4-7, 2000, IEEE, Perth, Western Australia, ISBN:0-7803-6338-8, pp: 1659-1664.

Krishna, C.K.A. and S.P. Deepthi, 2014. Analysis, simulation and comparison of various multilevel inverters using different PWM strategies. IOSR. J. Electr. Electron. Eng., 9: 54-65.

- Malinowski, M., K. Gopakumar, J. Rodriguez and M.A. Perez, 2010. A survey on cascaded multilevel inverters. *IEEE Trans. Ind. Electron.*, 57: 2198-2206.
- Peng, F.Z., 2001. A generalized multilevel inverter topology with self voltage balancing. *IEEE Trans. Ind. Applic.*, 37: 611-618.
- Priyan, S.S. and K. Ramani, 2013. Implementation of closed loop system for flying capacitor multilevel inverter with stand-alone Photovoltaic input. *Proceedings of the 2013 International Conference on Power, Energy and Control (ICPEC)*, February 6-8, 2013, IEEE, India, ISBN:978-1-4673-6027-2, pp:281-286.
- Rodriguez, J., J.S. Lai and F.Z. Peng, 2002. Multilevel inverters: A survey of topologies, controls and applications. *IEEE Trans. Ind. Electron.*, 49: 724-738.
- Sangolkar, H.S. and P.A. Salodkar, 2014. Comparative analysis of three topologies of three-phase five level inverter. *Intl. J. Sci. Eng. Technol.*, 3: 818-822.
- Shojaei, A., S.H. Fathi and N. Farokhnia, 2010. Power sharing improvement in cascaded multilevel inverters. *Proceedings of the 14th International Conference on Power Electronics and Motion Control (EPE-PEMC)*, September 6-8, 2010, IEEE, Ohrid, Macedonia, ISBN:978-1-4244-7856-9, pp: T3-88-T3-92.
- Sudarsanan, A., R. Roopa and S. Sanjana, 2015. Comparison of conventional and new multilevel inverter topology. *Intl. J. Sci. Eng. Res.*, 6: 330-334.