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Design and Implementation of Low Power Clock Gating Technique in 16 bit ALU Circuit

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Abstract: Power dissipation is the most important issues faced all the designers in modern science. Moreover, a clock pulse is a main reason of power consumption in digital design. Moreover, clock gating method in structure stage can be executed to decrease dynamic power. This study aim to design, implement and compare the various resources consumption utilizing clock gating techniques in 16 bit ALU design. The two clock signals proposed and used in the normal ALU design. Which supply the clock signal for one block only either logical or arithmetic block, while the other is switch OFF. With the purpose of executing arithmetic and logic architecture, 130 nm standard cell technology libraries are employed to realize the implementation. In addition, the simulations are compiled by using the Modelsim Software. Verilog Hardware Description Language (HDL) models is verified the construction of arithmetic and logic process. Similarly, it carried out with Quartus II 14.1 web edition (64 bit). This technique leads to the reduction in dynamic power consumption using AND based clock gating up to 32.88%. Therefore, the proposed design is acceptable to usage in the system to optimize power consumption in modern devices.

Key words: Clock gating, power dissipation, dynamic power, clock power, arithmetic, addition, verified

INTRODUCTION

The request, to decrease power consumption with high-performance in modern portables leads to the search for new techniques for decreasing power consumption in the digital design. Processors are represents the main parts of any digital computation device precise as of easiest implementations like information acquisition to the more complex like network on microchip NoC or system on microchip SoC. The mainframe unit which performs a logic as well as arithmetic functions wasted the large part of dissipated power compared with other peripheral devices. Therefore, the demands toward decreasing degenerate power are mine restrictions for all designers. All searching going on reducing power consumption in arithmetic and logic units is achieved and different methods of low power are offered. Therefore, power has come to be the vast task with realizing petty size and high performance design. This leads to the study indoors low power with high speed Very Large Scale Integrated Circuit (VLSI) systems. Power dissipation is estimated by different elements called the dynamic power, short circuit power and static power comprising the parameters that used to estimate total power consumption like frequency, switching activity, supply voltage and capacitor (Zhao *et al*., 2010). The general form to estimate equation of total power is known as:

$$P_{consumption} = P_{leakage} + P_{dynamic} + P_{shortcircuit} \quad (1)$$

The main part of power consumption is the switching power that is agreed as:

$$P_{dynamic} = C * \alpha * V2f \quad (2)$$

Where:

C = The capacitor measured (Mf)
α = The switching activity measured (MW)
V = The supply voltage as well as f is the frequency measured in MHz

Moreover, the techniques of power controller can be implementing at different stages in the system. The searching on design with reducing power is carried out at different levels like, architectural level, logical level, circuit level, technology level and at the system level. The surveys evidently designate the scale of power that is improved in system level is higher than the scale of power optimized at the transistor level. There are many approaches utilized to decrease power dissipation:

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optimized at the transistor level. There are many approaches utilized to decrease power dissipation: dynamic voltage and frequency scaling, multiple voltages, multiple thresholds, static voltage scaling, clock and logic power (Sahni *et al*., 2015). Every method has defiance with their execution. Furthermore, scientific designers implement less power design on a structure level of ALU. A system is validated by executing clock signal using AND based technique for power reduction. The ALU design is the synchronous system that's applied with pulse input. The clock signal in synchronous system dissipates much power than asynchronous system. From previous works, the clock consumes power up to 30% of power consumed in the system (Kathuria *et al*., 2011; Dev *et al*., 2013). Therefore, the demands to decrease it are challenging tasks for the designers. Clock gating method by means of AND based is applied to the design with power analysis for each scale of frequency.

MATERIALS AND METHODS

Technique of clock gating: Clock gating is the most popular way used in many synchronous designs for decreasing power consumption. Therefore, this technique saves more power by increase number of logic to the design to prune the clock tree. Clipping the clock inactive parts of the circuit, therefore the flip-flops in them don't switch on. It is an efficient way of decreasing power consumed in digital design. In synchronous model design like the basic target microprocessor, just part of the design is working at clock time. Therefore, by switching off the inactive part of the design, power dissipation can be saved (Soni and Hiradhar, 2015). One of the methods to realize this is by switch off the clock that goes to the inactive section of the design. Moreover, clock gating is an important procedure to decrease clock power in order to individual circuits used differs within and across applications. Not all the modules design is function during time operation giving rise to power lowering chance (Chaudhary *et al*., 2015). By adding clock with a gate en signal, CG technique ultimately inactive the clock design whenever the design is not necessary used to avoid power consumption generated from unimportant processes of the inactive design. Especially, CG technique goals the clock power dissipated in dynamic CMOS design realize for speed and area benefit over static logic. Operative clock gating technique however requires an organization that controls which module of design is gated when and for how long (Dev *et al*., 2013). CG technique is generated in repeated switching of the gated clock design among active then inactive states result in large overhead. In the same vein, the technique which uses small modules of the clock gating technique which is approximately as large as the modules themselves also lead to huge amount overhead. This overhead may result in power consumption which higher than that without clock gating (Aanandam, 2007). Moreover, clock gating is the methodology used in preventing the clock input from the target module which is inactive. This refers to switching off or inactivating the clock that is not important. There are different clock gating techniques applied to reduce power consumption during the modern time. Basically, to lower the magnitude of power consumption, switching activities on them must be reduced. This reduction can be realized through clock gating and clock frequency scaling (Czapski *et al*., 2007; Brynjolfson and Zilic, 2000). In clock gating technique, selected synchronous components of the design are out of action (disabled) by the way of removing the clock signal through inactive or sleep mode of operation (Zhang *et al*., 2006). The easiest way for clock gating techniques is by using a single AND gate with two input signals. The first one is the clock and the second one is the enabled signal. Nonetheless, this technique is not without drawbacks as will be discussed later. This technique will surely lead to setup and hold time violations in the circuit generated through improper alignment of the clock edges. Another technique is to use a flip flop to synchronize the enabled signal with the clock and reduce clock misalignment.

16 bit ALU implementation: This research presents a 16 bit ALU. The inputs a and b are of 16 bits with 16 bit output result also. The arithmetic and logic modules are executed as two functional blocks, logical and arithmetic unit. Arithmetic unit performed more than one function like subtraction, addition, increment and decrement and so on. The logical unit performed many logic operation like OR, NOT and Shift, XOR and XNOR and so on. The design utilizes selects lines every one for unit module. The ALU signified as two sectionsisexecuted utilizing with and without clock logic signal respectively. ALU design is simulated using ModelSim-Altera 10.3c (Quartus II 14.1) and implemented 130 nm technology library. The implementation process will explain in the next section.

ALU design: The ALU performs unary operations namely; complement, increment, decrement, logical shift

operations and binary operations namely: addition and subtraction which affect the flags. The sel [3:0] signal is used to select the required operation. Implementing the gated clock logic signal is stated according to the select lines, two inputs are estimated likewise the outcome is presented at ALU_out and ALU generates respective flags. The operations selected depending on various select lines are shown in Table 1.

ALU design with clock gating: The procedures that put the idle components in OFF mode are called clock gating technique. In the circuit work by clock signal, the clock is applied to all elements of design. In the implementation mode not all are functioning. Hence, those components or a design that is not functioning while consume power. Therefore, clock signal method is executed where a target clock can no present immediately to entirely the clocked plan but by way of an enable signal. In this methodology and based procedure is implemented. Figure 1 shows AND based CG.

The control clock is fed to the design. The procedure to achieve this goalif the en signal is zero, the clock is gated to the first AND gate to the logic unit. When en signal is one, the clock is gated to the second AND gate to Arithmetic unit. Hence, at one time the gated clock output is active only shown in Table 2.

Table 1: Select line operations

operations	S_0	S_1	S_2	S_3
And	0	0	0	0
NAND	1	0	0	0
NOR	0	1	0	0
BUFFER A	1	0	0	0
EX-OR	1	1	0	0
BUFFER B	0	1	0	0
EX-NOR	1	1	1	0
ADDITION	0	0	0	1
ENCREMENT	1	0	0	1
2_S COMPLEMENT	0	1	0	1
SET	1	1	0	1
SUBSTRACTION	0	0	1	1
DECREMENT	1	0	1	1
NOT	0	1	1	1
CLEAR	1	1	1	1

Table 2: Activating of signal en

Values	Variables
Activation	en
Logic unit	0
Arithmetic unit	1

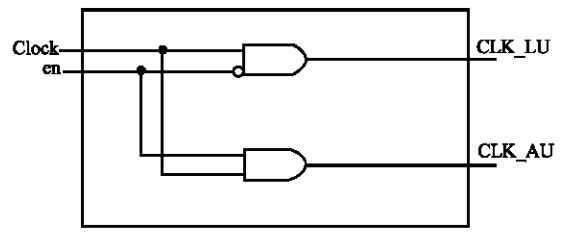

Fig. 1: AND based CG design

In Fig. 2 when en is zero, the output of multiplexer is obtained from the logic module also when en set to one, the output is obtained from the arithmetic module. Moreover, the chose output is produced during the output register clocked by the gated clocks. Figure 3 shows the RTL viewer of top-level ALU with CG.

The inputs clk and en are ANDed and the output clkg is the clock input to the clocked design. The code is optimized and simulated ModelSim-Altera 10.3c (Quartus II 14.1). The power due to the switching activity of the inputs, select line and the outputs are measure. Technology map viewer of 16 bit ALU connected to clock signal is shown in Fig. 4.

When the compilation and synthesis processes are perform the RTL illustration is estimated whic is included the standard cells. The device utilization of the design of ALU with and without CG is tabulated in Table 3 and 4.

Table 3: Device utilization without C

Recourses	Used	Available	Utilized (%)
Total logic elements	550	21.280	3
Total combinational functions	550	21.280	3
Dedicated logic registers	32	21.280	<1
Total registers	32	-	-
Total pins	69	16.7	42

Table 4: Device utilization with C

Recourses	Used	Available	Utilized (%)
Total logic elements	279	21.280	1
Total combinational functions	279	21.280	1
Dedicated logic registers	32	21.280	<1
Total registers	32	-	-
Total pins	70	16.7	42

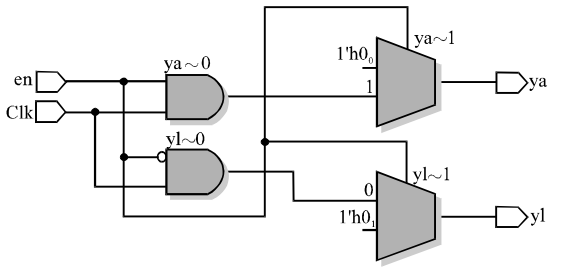

Fig. 2: RTL viewer of clock gating module MUX

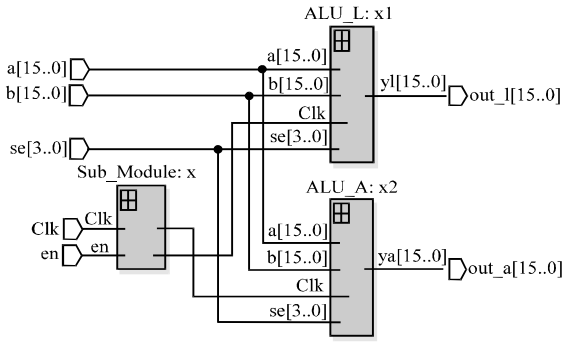

Fig. 3: RTL viewer of top-level ALU with CG

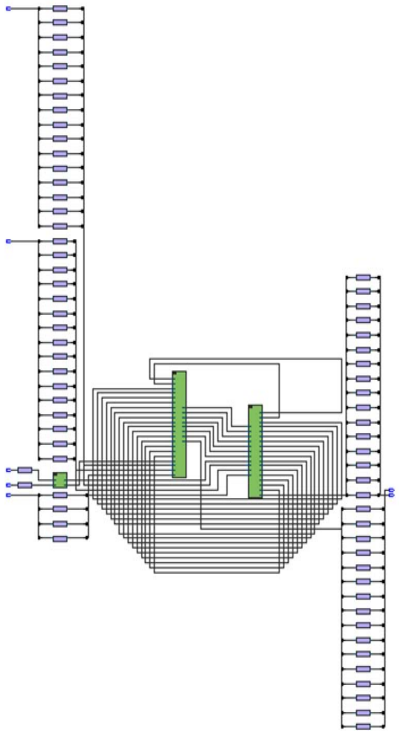

Fig. 4: Technology map viewer of ALU design

RESULTS AND DISCUSSION

The circuit of ALU design with CG and without CG is executed utilizing the Verilog HDL coding, validated utilizing ModelSim-Altera 10.3c (Quartus II 14.1). The power analyses using 130 nm technology library. The validated output signal is shown in Fig. 5.

From the validated output waveform, clear recognized that the producing varieties while the trigger pulse is clocked. The performing process for logical or arithmetic is not checking at this time but each of the processes is done. Through implementing the en clock signal gating, the en signal is utilized for choose any process is to be executed consequently just one operative module will get the pulse signal as well as the second module will not clocked. Therefore, the power in the unnecessary module is reserved. The validation of en signal ALU is shown in Fig. 6. By noticed in the validation outcome the result is realized while the identical target module is clocked like. Once the arithmetic operation is clocked, the clock gated signal is connected only with arithmetic part whereas the outcome of the logical process will be equivalent such as that of the achievement performance at last steps. The analysis of power design using gated clock and without using gated clock is done utilizing 130 nm technology libraries.

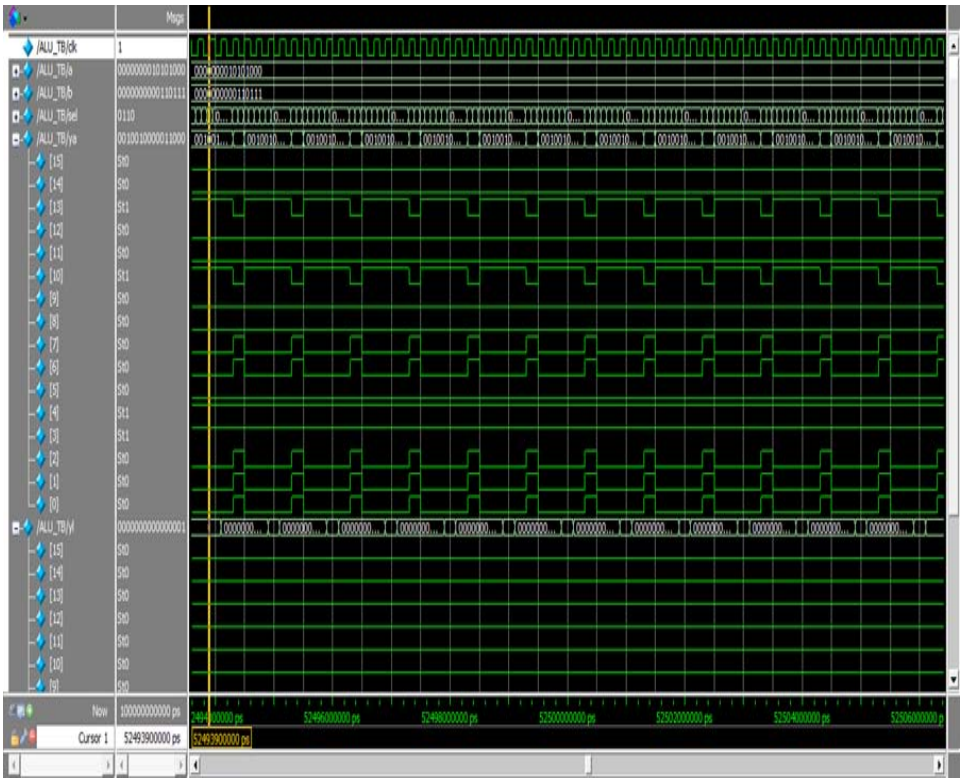

Fig. 5: Waveform of ALU design without CG

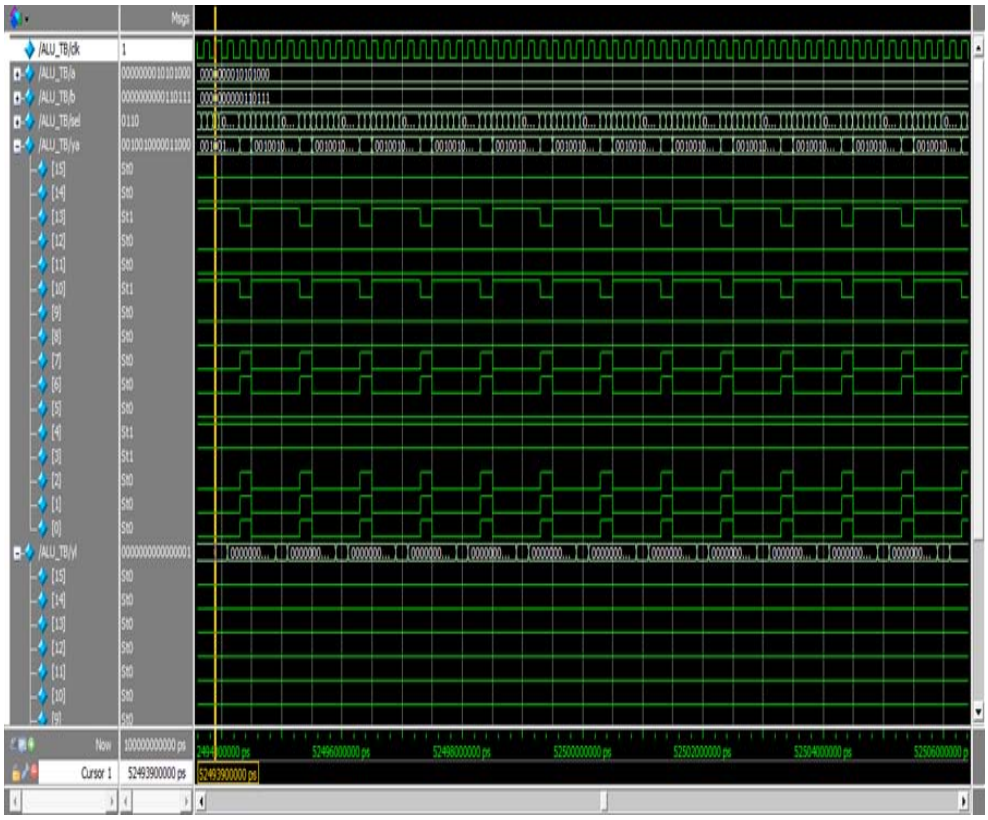

Fig. 6: Validation output design with enable CG

Table 5: Power ALU without CG

Frequency (MHz)	Time (NS)	Dynamic (MW)	Leakage (MW)	Total (MW)
100	10	0.20360	0.0001	0.2044
200	5	0.52460	0.0001	0.5259
300	3.3333	0.08975	0.0001	0.8990
500	2	1.57660	0.0001	1.5781
800	1.25	2.50030	0.0001	2.5017
1000	1	3.11150	0.0001	3.1128

Table 6: ALU with CG

Frequency (MHz)	Time (NS)	Dynamic (MW)	Leakage (MW)	Total (MW)
100	10	0.1658	0.0011	0.1670
200	5	0.4330	0.0011	0.4345
300	3.3333	0.6420	0.0013	0.6435
500	2	1.0992	0.0013	1.1006
800	1.25	1.7264	0.0039	1.7278
1000	1	2.0894	0.0036	2.0908

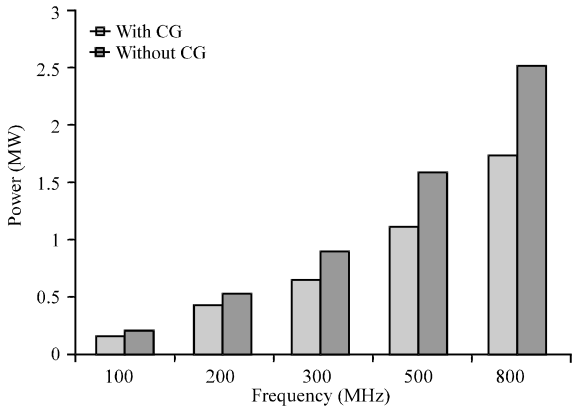

Fig. 7: Variation power with frequency

ALU design without clock gating: The report of power consumption is completed when the input clock gating signal is providing to each of the modules. The estimated and total results for dynamic power and for various frequencies are defined and listed in Table 5. The determination of power consumption is in MW while the frequency in MHz. As of the results, it is realized that the dynamic power consumption increases with increasing frequency. Meant to lowering frequencies, dynamic power dissipation modifications are lower, conversely for highest frequencies, the difference is in height as the clock signal goes beyond the named frequency that outdoes the junction temperature (Fig. 7). On implementing the en gating signal, the power dissipated by the clock decreases. Table 6 presents the power dissipation of the design using clock gating.

CONCLUSION

Power dissipation in modern devices is an increasing concern as requests for extended battery life lowering heat radiation and improved device reliability is on the rise. After implementing clock power to a 16 bit ALU, there is a saving in a dynamic power and total power consumption. In this research, the power optimization at architectural level is validated by the design using AND based clock gating techniques. It is noted that clock gating decreases dynamic power consumption of the design by approximately 32.83%. The ALU is capable of executing fifteen processes and can be readily sited in the data path of a 16 bit microprocessor.

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