Journal of Engineering and Applied Sciences 13 (8): 2042-2048, 2018
ISSN: 1816-949X

Design and Implementation of Area Efficient Reversible Full Adder-Subtractor in QCA

[1]Sharmin Farzana, [1]Ali Newaz Bahar, [1]Nur Mohammad Nahid and [2]Abdul Mohaimin Eusufzai
[1]Department of Information and Communication Technology (ICT),
Mawlana Bhashani Science and Technology University (MBSTU),
Santosh, 1902 Tangail, Bangladesh
[2]Institute of Information Technology, Jahangirnagar University, Savar, 1342 Dhaka, Bangladesh

Abstract: In the near future, the part of energy dissipation due to information loss in irreversible computation will become a serious issue in VLSI chips. A Quantum-dot Cellular Automata (QCA) is anemerging nanotechnology which facilitates reversible computing. It's a new computing paradigm with applications in extremely low energy dissipation. In this study reversible full adder-subtractor is proposed. For evaluating the functionality and energy dissipation QCA Designer and QCAPro tools are used. Proposed design is implemented in multi-layer in QCA designertool. It improves 78% of cell count compared to the existing QCA-based reversible full adder-subtractor. QCAPro tool demonstrates the efficiency of leakage and switching energy improvements.

Key words: Quantum-dot cellular automata, reversible computing, full adder-subtractor, single layer circuit, multi-layer circuit, reversible

INTRODUCTION

Nanotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among these new devices, Quantum-dot Cellular Automata (QCA) (Lent *et al*., 1994; Smith, 1999) operates new physical phenomena and innovative techniques that depart from a CMOS-based model. QCA gives a solution at nano-scale and it also offers a new method of computation and information (Amlani *et al*., 1998; Orlov *et al*., 1997).

In modern VLSI system, the power consumption is the main concern. The disproportionate scaling of the size of transistors and power supply voltage has led to high leakage currents and high power density creating hot spots in CMOS chips. For this reason,different computational paradigms by using nanotechnologies, addressing small size and low power dissipation should be considered. Reversible computing is a computational paradigms which is a one-to-one mapping between the input and output states of the circuit (Ma *et al*., 2008; Sen *et al*., 2014).

The first 1 bit full adder in QCA wasproposed by Tougaw and Lent (1994). This design is constructed using five-threeinput majority gates and three inverters. However, a simpler QCA full adder was presented (Wei *et al*., 2003). This full adder is composed of three-three input majority gates and two inverters. Different layouts for a QCA full adder have been presented using this design (Zhang *et al*., 2004). Then, anovel QCA full adder design was introduced (Azghadi *et al*., 2007). This design is composed of one three input majority gates, one inverter and a new kind of majority gate, a five input voterare used only for its advantages in wire crossing (Hashemi *et al*., 2012; Cho and Swartzlander, 2007; Pudi and Sridharan, 2012). A new five-input majority gate (5 MV) is proposed and a new full adder based on that 5 MV is synthesized (Hashemi *et al*., 2012). After that adder, subtractor is designed (Sangsefidi *et al*., 2015) which is 8 bit. A multilayer 1-bit Full-Adder (FA) is designed (Bahar *et al*., 2014).This design presents a single layer five-input Majority Voter gate (MV5) and power dissipation are estimated.

For the design of many computation systems and functional circuits adder and subtractor are used. Different kinds of half/full adder designs with different number of majority gates are presented (Kim *et al*., 2007; Ahmad *et al*., 2014a-c; Safavi and Mosleh, 2013; Santra and Roy, 2014) and the full adder design proposed has better performance.

A small number of QCA based binarysubtractors have been proposed. Full adder and full subtractor designed (Ahmad *et al*., 2014a-c) present less area, circuit complexity and clock delays. Fredkin (Bahar *et al*., 2015) and Feynman (Bahar *et al*., 2014) gates based different binary subtractors have been proposed (Thapliyal *et al*., 2005). For employing half subtractor, the design proposed

Corresponding Author: Ali Nawaz Bahar, Department of Information and Communication Technology (ICT), Mawlana Bhashani Science and Technology University (MBSTU), Santosh, 1902 Tangail, Bangladesh

(Lakshmi *et al*., 2010; Srivastava *et al*., 2011) has required 77 and 55 cells. Reshi has proposed a half and full subtractors that require 45 and 104 cells, respectively for implementation (Srivastava *et al*., 2011). Most recently, 2-input XOR gate based half and full subtractors (Bahar *et al*., 2017) have been proposed which required 19 and 32 cells, respectively.

Reversible Quantum Gate (RQG) is proposed (Moaiyeri *et al*., 2016). This design is proposed reversible full adder subtractor using RQG gate in single layer. This designimproves the cell count and area.

In this study, reversible full adder-subtractor is proposed which is implemented in multi-layer using RQG gate. It has significantly lower number of cells and smaller area even in comparison with its single layer and multilayer counterparts.

Overview of QCA: One of the most attractive and promising nanotechnologies is Quantum-dot Cellular Automata (QCA). It operates based on Coulombic interactions (Ma *et al*., 2008; Roohi *et al*., 2015). In QCA, two electrons inside the cell determine the '0' and '1' logics as shown in Fig. 1a. The electrons moves quantum-mechanically tunnel between the dots though tunneling junctions and fix either with cell polarization in P = 1 (logic1) or P = -1 (logic 0) as illustrated in Fig. 1a.

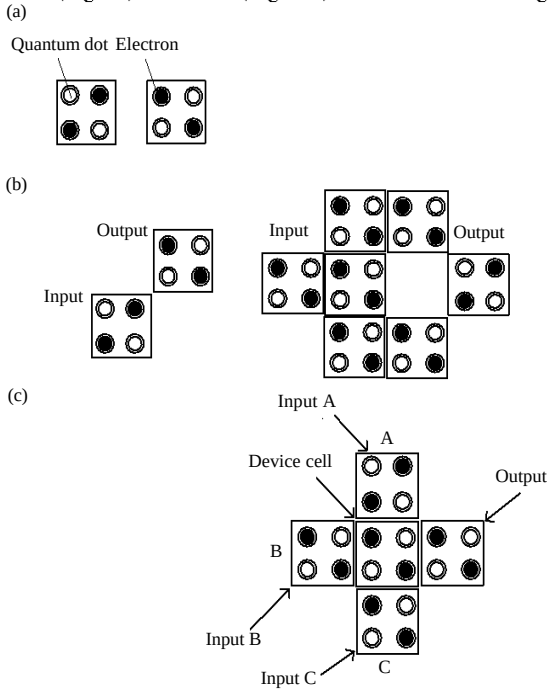

Fig. 1: QCA logic; a) QCA cells; b) QCA inverter and c) QCA three-input majority gate

During the state transition and propagation, there is no energy dissipation in QCA. So, QCA dissipates extremely lower power compared to the CMOS technology. The energy dissipated per switching event in a reversible QCA circuit can be significantly less than kBTln2 due to clocked information-preserving system. Implementing efficient reversible logic gates become possible using QCA (Timler and Lent, 2002).

Figure 1b and c show the fundamental QCA gates, the inverter and the Majority (MAJ) gates. The QCA inverter is usually realized in two different configurations reverses the cell polarization and the output of the majority gate will be the majority of the inputs.

MATERIALS AND METHODS

Proposed designs: Reversible Quantum Gate (RQG) is proposed in this study. RQG gate a 3×3 reversible logic gate. According to Eq. 1-3, this gate has three inputs A, B and Cand generates three outputs P, Q and R. In Table 1, truth table showsthatthe RQG gate is fully reversible with a completely one-to-one mapping between the inputs and outputs. Figure 2 is shown the proposed reversible gate:

$$P=MAJ(A,B,C)=A.B+B.C+A.C \quad (1)$$

$$Q=MAJ(A',B,C)=A.B+B>C+A'C \quad (2)$$

$$R=A\oplus C=A.C'+A'C \quad (3)$$

To implement and verify all of the designs in this study, the QCA designer tool has been used. In Fig. 3, RQG is shown the QCA layout of the proposed reversible gate. The RQG gate is composed of two three-input majority gates and one 2-input exclusive OR (XOR) gate. Figure 4 shows the simulation result of RQG. It shows the correctness of truth table.

Proposed reversible full adder-subtracter: The RQG gate can be used to implement important logic circuits such as

Table 1: Truth table of proposed gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

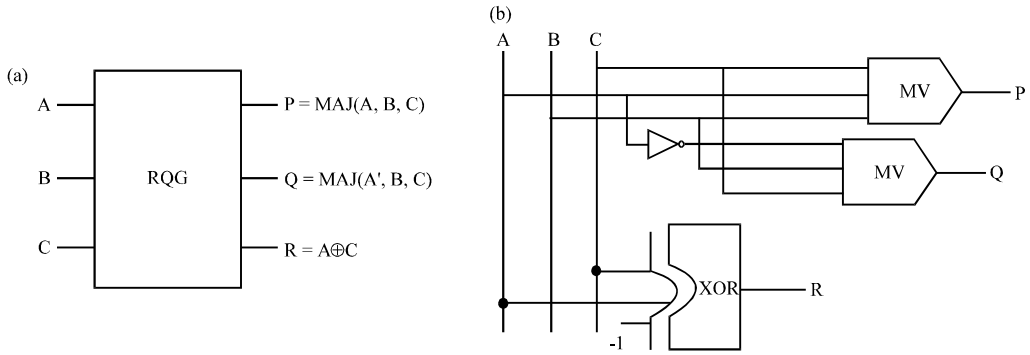

Fig. 2: The proposed reversible gate; a) Block diagram and b) Schematic diagram

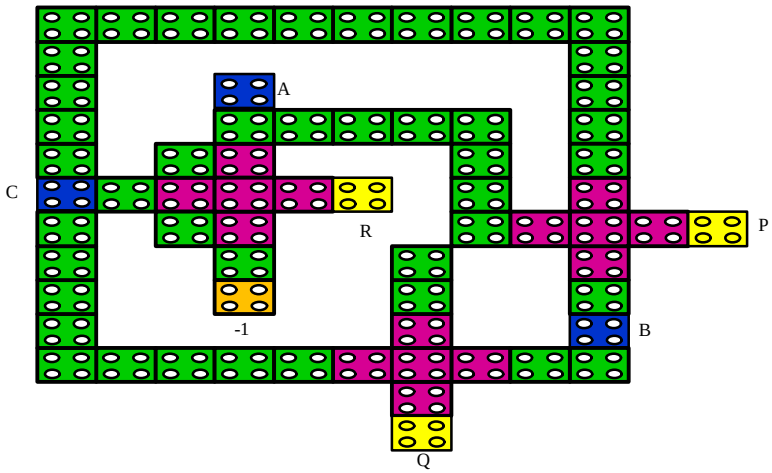

Fig. 3: Layout of the proposed Reversible Quantum Gate (RQG)

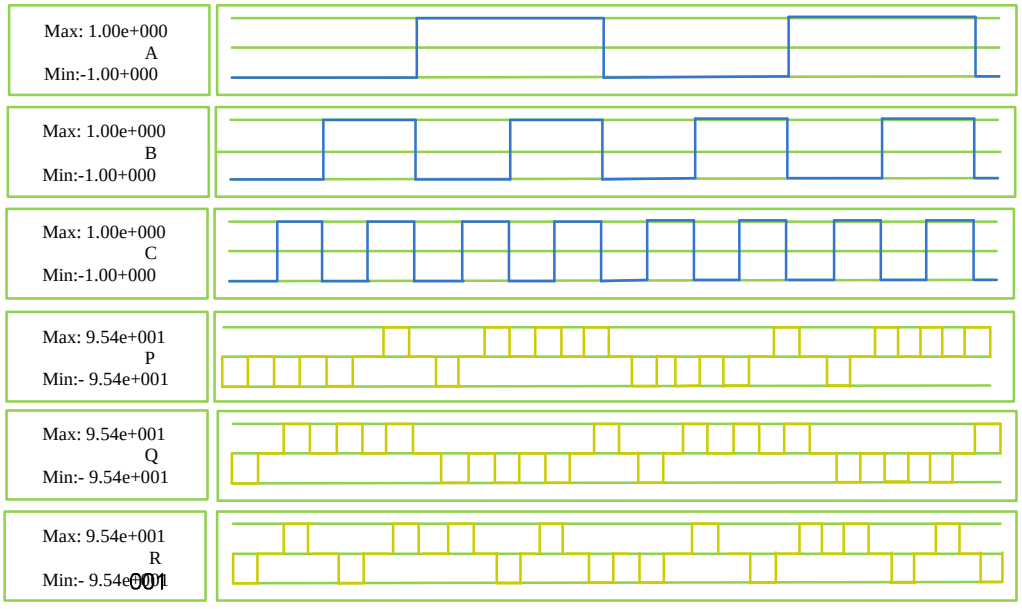

Fig. 4: Simulation result of RQG

full adder and full subtractor. By using an RQG and two Feynman (FG) reversible gates, an efficient reversible full adder-subtractor circuit with four inputs and four outputs is proposed which is shown in Fig. 5. A Feynman gate with x and y inputs, provides x and ⊕ outputs (Ma *et al*., 2008). In the proposed design, the first FG replicates the B input and the second one is used to create a three input XOR (A⊕B⊕C). The three main outputs of the circuit provides the full adder-subtractor as given in Eq. 4-6 where Sum and Diff are the sum and difference of the three inputsand Cout and Bout are the output carry and borrow, respectively. Furthermore, the forth output (A⊕C) is a garbage output.

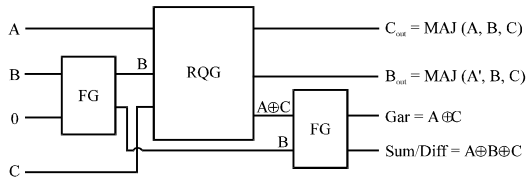

Fig. 5: Proposed reversible full adder-subtractor

The layout of the proposed full adder-subtractor is designed using three layers of QCA cells. Figure 6 shows the QCA implementation of full adder-subtractor. It shows three different layers that indicate the main layer, layer-1 and layer-2. The layout of proposed multi-layer full adder-subtractorshows in Fig. 6d in Top view. This design enhances the robustness and manufacturability of the proposed design. Table 2 presents truth table of the proposed design.

Simulation results and comparisons: A popular simulation tool named QCADesigner is used for simulation and verification of the designs. The simulation

Table 2: Truth table of the proposed reversible full adder-subtractor

A	B	0	C	Cout	Bout	Sum/Diff	Gar
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	1	0	0	0	1	1	0
0	1	0	1	1	1	0	1
1	0	0	0	0	0	1	1
1	0	0	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0

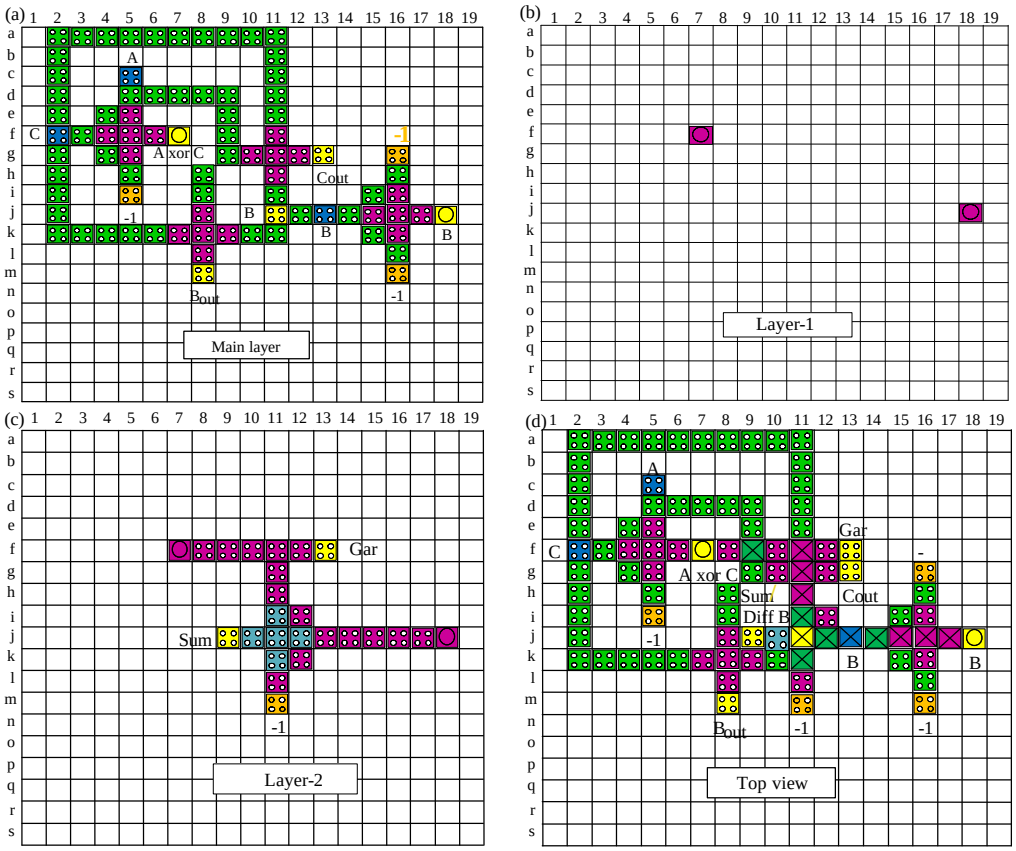

Fig. 6: QCA implementation of the proposed full adder-subtractor; a) Main layer; b) Layer-1; c) Layer-2 and d) Top view

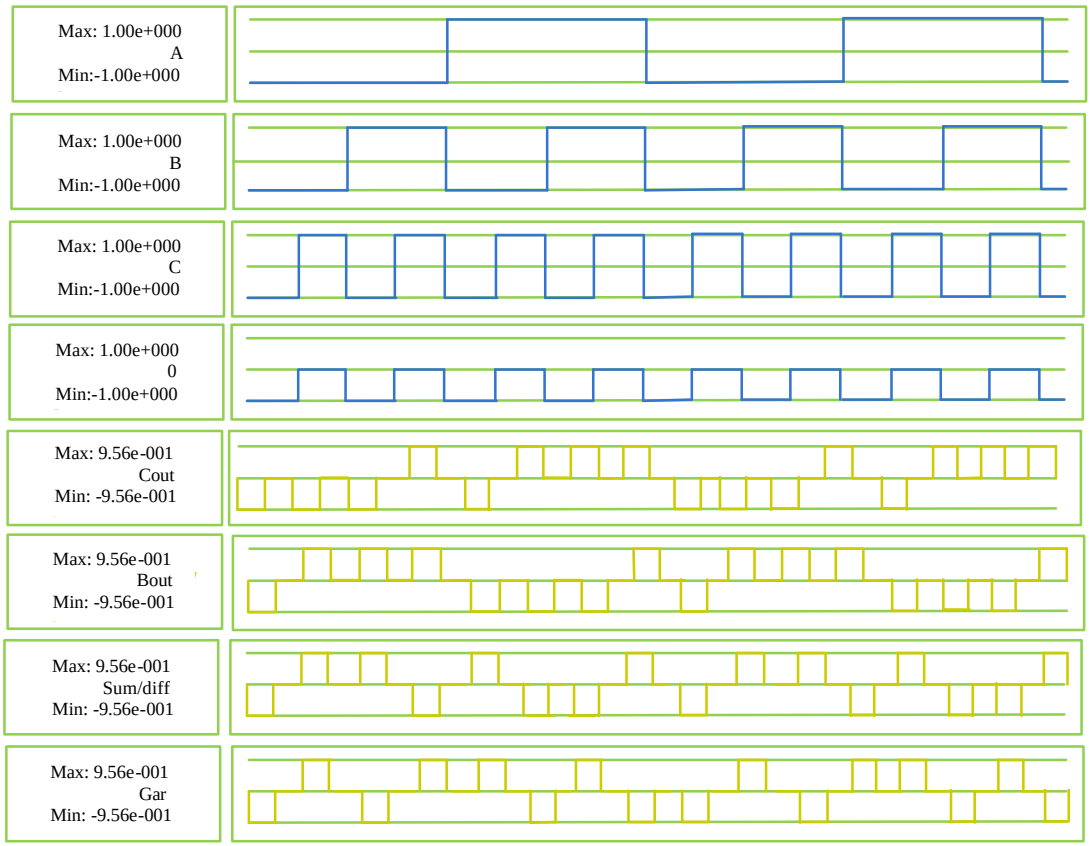

Fig. 7: Simulation results of the proposed full adder-subtractor

Table 3: Comparison of reversible QCA full adders

Categories	Cells	Layers	Area (μm^2)	Latency (clock cycles)	Garbage outputs
QCA (Lent *et al*., 1994)	343	1	0.46	1.50	3
QCA2 (Lent *et al*., 1994)	356	1	0.47	1.50	3
FG+RQCA (Smith, 1999)	517	1	0.78	3.25	2
Proposed	113	3	0.10	1.25	1

results shown in Fig. 7 claim the functionality of the proposed multi-layer reversible full adder-subtractor which utilizes the RQG gate as its main block.

Table 3 shows a comparison between our proposed full adder-subtractor design and existing reversible designs. The proposed reversible full adder-subtractorproduces only one garbage output which is fewer than the other designs. Using different clock zones for wire crossing makes the latency (number of clock cycles) of the proposed design slightly shorter than others. Our proposed design is multi-layer without any rotated cellswhich significantly enhance its robustness and manufacturability and it performs both addition and subtraction operations. It has considerably lower number of cells and much smaller area in comparison with both single-layer and multilayer designs.

Energy analysis: To evaluate consumed power of the proposed design, we use QCAPro (Saket *et al*., 2011) tool. QCAPro is an acceptable power valuator tool that estimate energy dissipation of proposed circuits. In three different tunneling energy levels 0.5 E_k, 1 E_k 1.5 E_k at 2 K temperature, the energy dissipation is analyzed. Energy dissipation analysis of proposed multi-layer reversible full adder-subtractor at three different tunneling energy levels is shown in Table 4. This table shows leakage energy dissipation, switching energy dissipation and total energy dissipation. The graphical presentation of energy dissipation of proposed full adder-subtractor is shown in Fig. 8.

The power dissipation maps of presented reversible full adder-subtractor are shown in Fig. 9. In this figure, it is clear that high power dissipating cells are indicated with darker colors.

Reliability analysis: Reliability analysis is the temperature effect on Average Output Polarization (AOP) of proposed gates has been analyzed by QCA designer and the maximum and the minimum polarizations for each output cell are observed. The output polarizationof cell is taken

Table 4: Energy dissipation analysis of proposed full adder-subtractor

	Leakage energy dissipation (meV)			Switching energy dissipation (meV)			Total energy dissipation (meV)		
Circuit	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
Multilayer full adder-subtractor	55.67	137.9	239.18	94.75	83.16	72.86	150.42	221.06	312.04

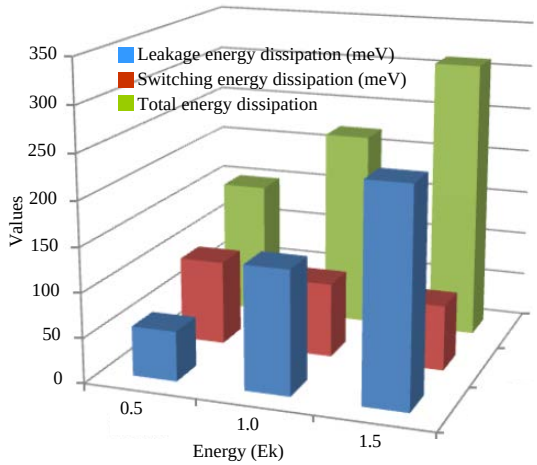

Fig. 8: Energy dissipation of proposed full adder subtractor

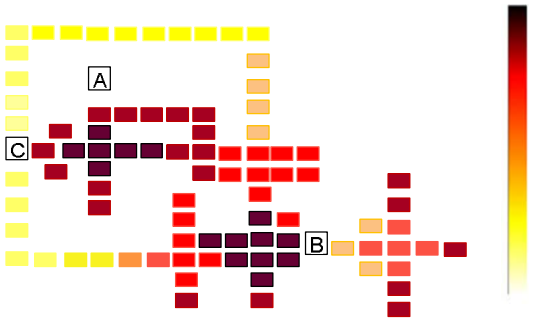

Fig. 9: Power map of proposed reversible full adder subtractor

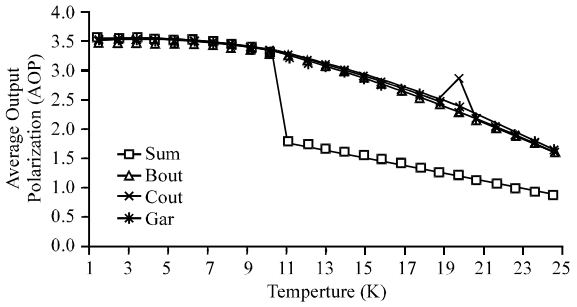

Fig. 10: Effect of temperature on average output polarization of proposed QCA circuit

at different temperature. The AOPs for different output cells of proposed layout at different temperatures are calculated and plotted in Fig. 10. The AOP of the output cells Sum/Diff and Gar of the reversible full adder-subtractor is gradually decreased, up to a temperature of T = 7 K as shown in Fig. 10. Thus, in between temperatures 1 and 7 K, sum/diff and gar works efficiently. Above the temperature T = 7 K, the AOP falls down radically and produces inconsistent outputs. The output Bout and Cout remain constant. When the temperature is above 32 K, the AOP is dropped drastically which results incorrect outputs.

CONCLUSION

This study presents an efficient QCA-based multi-layer reversible full adder-subtractor for reversible nanocomputing which provides with both addition and subtraction operations. It has multi-layer structure in terms of cell count area, it outperforms the previous reversible full adder. It improves 78% cell count and 87% area compared to others. The leakage and switching energydissipations in these designs are calculated by using QCAPro tool. In addition, it does not require rotated cells and has a lower number of garbage outputs requiring less power dissipation.

REFERENCES

Ahmad, F., G.M. Bhat and P.Z. Ahmad, 2014a. Novel adder circuits based on Quantum-Dot Cellular Automata (QCA). Circuits Syst., 5: 1-11.

Ahmad, P.Z., F. Ahmad and H.A. Khan, 2014b. A new F-shaped XOR gate and its implementations as novel adder circuits based Quantum-dot cellular Automata (QCA). IOSR. J. Comput. Eng., 16: 110-117.

Ahmad, P.Z., F. Ahmad, S.M. Ahmad and R.A. Khan, 2014c. Implementation of quantum dot cellular automata based novel full adder and full subtractor. Intl. J. Sci. Res., 3: 573-577.

Amlani, I., A.O. Orlov, G.L. Snider, C.S. Lent and G.H. Benstein, 1998. Demonstration of a six-dot quantum cellular automata system. Applied phys. Lett., 72: 2179-2181.

Azghadi, M.R., O. Kavehei and K. Navi, 2007. A novel design for quantum-dot cellular automata cells and full adders. J. Applied Sci., 7: 3460-3468.

Bahar, A.N., S. Waheed and M.A. Habib, 2014. A novel presentation of reversible logic gate in Quantum-dot Cellular Automata (QCA). Proceedings of the 2014 International Conference on Electrical Engineering and Information and Communication Technology (ICEEICT), April 10-12, 2014, IEEE, Tangail, Bangladesh, ISBN:978-1-4799-4820-8, pp: 1-6.

Bahar, A.N., S. Waheed and M.A. Habib, 2015. An efficient layout design of fredkin gate in Quantum-dot Cellular Automata (QCA). Duzce Univ. Sci. Technol. Rev., Vol. 3,

Bahar, A.N., S. Waheed, N. Hossain and M. Asaduzzaman, 2017. A novel 3-input XOR function implementation in quantum dot-cellular automata with energy dissipation analysis. Alexandria Eng. J., Vol. 2017,

Cho, H. and E.E. Swartzlander, 2007. Adder designs and analyses for quantum-dot cellular automata. IEEE Trans. Nanotechnol., 6: 374-383.

Hashemi, S., M. Tehrani and K. Navi, 2012. An efficient Quantum-Dot Cellular Automata full-adder. Sci. Res. Essays, 7: 177-189.

Kim, K., K. Wu and R. Karri, 2007. The robust QCA adder designs using composable QCA building blocks. IEEE Trans. Comput. Aided Design Integ. Circuits Syst., 26: 176-183.

Lakshmi, S.K., G. Athisha, M. Karthikeyan and C. Ganesh, 2010. Design of subtractor using nanotechnology based QCA. Proceedings of the 2010 IEEE International Conference on Communication Control and Computing Technologies (ICCCCT), October 7-9, 2010, IEEE, Salem, India, ISBN:978-1-4244-7769-2, pp: 384-388.

Lent, C.S., P.D. Tougaw and W. Porod, 1994. Quantum cellular automata: The physics of computing with arrays of quantum dot molecules. Proceedings of the Workshop on Physics and Computation (PhysComp'94), November 17-20, 1994, IEEE, Notre Dame, Indiana, ISBN:0-8186-6715-X, pp: 5-13.

Ma, X., J. Huang, C. Metra and F. Lombardi, 2008. Reversible and Testable Circuits for Molecular QCA Design. In: Emerging Nanotechnologies, Tehranipoor, M. (Ed.). Springer, New York, USA., ISBN:978-0-387-74746-0, pp: 157-202.

Orlov, A., G. Amlani Bernstein, C. Lent and G. Snider, 1997. Realization of a functional cell for quantum-dot cellular automata. Science, 277: 928-930.

Pudi, V. and K. Sridharan, 2012. Low complexity design of ripple carry and Brent-Kung adders in QCA. IEEE. Trans. Nanotechnol., 11: 105-119.

Roohi, A., H. Thapliyal and R.F. DeMara, 2015. Wire crossing constrained QCA circuit design using bilayer logic decomposition. Electron. Lett., 51: 1677-1679.

Safavi, A.A. and B.M. Mosleh, 2013. An overview of full adders in QCA technology. Intl. J. Comput. Sci. Eng., 1: 12-35.

Sangsefidi, M., M. Karimpour and M. Sarayloo, 2015. Efficient design of a coplanar adder-subtractor in Quantum-dot Cellular Automata. Proceedings of the 2015 IEEE Symposium on European Modelling (EMS), October 6-8, 2015, IEEE, Mashhad, Iran, ISBN:978-1-5090-0207-8, pp: 456-461.

Santra, S. and U. Roy, 2014. Design and implementation of quantum cellular automata based novel adder circuits. Intl. J. Comput. Electr. Autom. Control Inf. Eng., 8: 1-6.

Sen, B., M. Dutta, S. Some and B.K. Sikdar, 2014. Realizing reversible computing in QCA framework resulting in efficient design of testable ALU. ACM. J. Emerging Technol. Comput. Syst., Vol. 11, 10.1145/2629538

Smith, C.G., 1999. Computation without current. Sci., 284: 274-274.

Srivastava, S., A. Asthana, S. Bhanja and S. Sarkar, 2011. QCAPro-an error-power estimation tool for QCA circuit design. Proceedings of the 2011 IEEE International Symposium on Circuits and Systems (ISCAS), May 15-18, 2011, IEEE, New Delhi, India, ISBN:978-1-4244-9473-6, pp: 2377-2380.

Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005. Reversible logic synthesis of half, full and parallel subtractors. Proceedings of the 2005 International Conference on Embedded Systems and Applications (ESA 2005), June 27-30, 2005, CSREA Press, Las Vegas, Nevada, ISBN:1-932415-53-X, pp: 231-237.

Timler, J. and C.S. Lent, 2002. Power gain and dissipation in quantum-dot cellular automata. J. Appl. Phys., 91: 823-831.

Tougaw, P.D. and C.S. Lent, 1994. Logical devices implemented using quantum cellular automata. J. Applied Phys., 75: 1818-1825.

Wei, W., K. Walus and G.A. Jullien, 2003. Quantum-dot cellular automata adders. Proceedings of the 3rd Conference on Nanotechnology, August 12-14, 2003, IEEE Xplore, London, pp: 461-464.

Zhang, R., K. Walnut, W. Wang and G. Jullien, 2004. A method of majority logic reduction for quantum cellular automata. IEEE Trans. Nanotechnol., 3: 443-450.