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# Implementation of Single Phase Cascaded H-Bridge Inverter System

D. Karthikeyan, R. Palanisamy, K. Selvakumar, D. Selvabharathi and K. Vijayakumar
Department of Electrical and Electronics Engineering (EEE), SRM University, Chennai, India

**Abstract:** This study presents a 5-level single phase cascaded H-bridge multilevel inverter where in two H-bridges are in series and there are separate DC voltage source for each H-bridge. The modulation technique we have used is sinusoidal pulse width modulation because it helps in reducing the unwanted harmonics. A single phase cascaded H-bridge multilevel inverter model is presented in this studyand performance of this inverter is investigated through various simulation studies using MATLAB/Simulink. The simulation result shows the effective control to obtain minimum THD performance. Potential drawbacks of conventional inverters are eliminated here.

**Key words:** Cascaded H-bridge inverter, Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD), DC voltage, inverters, pulse

## INTRODUCTION

In the present era due to blistering development, energy which plays a crucial role in both economic as well as human development can be found throughout the globe. Due to enormous technology, we often need power in some manageable form and this is made possible through an inverter (a device which converts AC to DC). It is an essential power electronic device which has immense application in fields like powerbackup, solar panel, fuel cells, etc., a general power electronic inverter has two levels of voltage i.e., it divides the input voltage ($V_{dc}$) into two levels ($+V_{dc}/2$ and-$V_{dc}/2$) in order to build an AC voltage and although, it creates AC voltage but it is not a perfect sinusoidal waveform and has limitations like harmonic distortion, limited voltage applications, higher switching losses, high electromagnetic induction, etc.

So, in order to overcome these limitations we usea high power, high voltage and low harmonic distortion device, i.e., a multilevel inverter which produces the desired AC output voltage from various lower DC voltages (Thongprasri, 2011).We prefer it because it produces output in step staircase form. It has advantages like lower total harmonic distortion, reduced switching stress, high voltage applications, low electromagnetic induction and less switching frequency (Haw *et al*., 2015). Mostly in conventional multilevel inverters, many semiconductor switches and regulated gate driver circuits are required which increase the overall expense and complexity. Thereby, in this study a new topology is suggested with higher levels and lower number of switches (Palanisamy *et al*., 2016a, b).

Now, the total harmonic distortion of a device is inversely proportional to number of voltage levels but as we increase the number of voltage levels the hardware and complexity of the project device increases and so, increases the price and weight. Therefore, we have to trade off between price, weight, complexity and the total harmonic distortion, therefore, in this study we are going for a 5 level multilevel inverter.There are several topologies of multilevel inverter like diode clamped (Corzine *et al*., 2004) flying capacitor and cascaded H bridge structures (Peng, 2000).Diode clamped multilevel inverter is known as neutral point inverter because when it was used in a three level inverter the mid voltage level was defined as the neutral point level (Manjrekar *et al*., 2000). The basic concept behind the use of diodes is to limit the voltage stress on power devices wherein capacitor can be pre-charged together at the desired voltage level. The capacitor requirement of the inverter is minimized due to all phase sharing a common DC link. The output voltage distortion is very low due to multiple levels in the output voltages (Palanisamy *et al*., 2015).

But the maximum output voltage is half of the input DC voltage which is the main drawback and moreover charge balance gets disturbed for more than three level intermediate DC levels tend to be whenever without the appropriate control making the real power transmission a problem (Lee *et al*., 2015). Flying capacitor multilevel inverter is also known as “Imprecated Cell Inverter”. It is quite similar to the diode clamped multileveled inverter but unlike diode clamped the main concept of this inverter is to use capacitor for clamping and is known as flying capacitor because the capacitor float with earth’s

**Corresponding Author:** D. Karthikeyan, Department of Electrical and Electronics Engineering (EEE), SRM University, Chennai, India

potential (Kouro *et al*., 2008). If the input voltage is $V_{DC}$ then the output voltage is $V_{DC}/2$, i.e., half and this is the major drawback of this type of capacitors. It can control both active and reactive power flow but due to the high frequency switching, switching losses will take place (Palanisamy *et al*., 2016a, b). An 'n' level inverter needs:

- No. of voltage source NDC = (n-1)
- No. of switching devices NSD = 2(n-1)
- No. of balancing capacitors NBC = (n-1)*(n-2)/2

Generally, transistor are used as switching device in flying capacitor which are placed nearer to the source voltage ($V_{dc}$) having higher voltage in comparison to the capacitors nearer to load.

## MATERIALS AND METHODS

### Cascaded H-bridge inverter

**H-bridge:** The combinations of capacitors and switches pair are called an H-bridge and separate input DC voltage is present for each H-bridge. Each cell can provide three different voltages like 0, +DC, -DC. H-bridge is basically simple circuits have the configuration of the english alphabet H where there are four switching elements and the load is presented in the center. A cascaded H-bridge cell is also called a full bridge inverter. The basic idea behind this invertor is to get a sinusoidal voltage output by connecting H-bridge inverter in series. In cascaded H Bridge, the power drain requirements vary from voltage level to voltage level. Therefore, different separate DC sources must be used for each H-bridge in such a manner that the power requirements are met for each level. Cascaded multilevel inverter has high power applications in shunt and series connected facts controllers.

The cascaded H-bridge can be either asymmetrical or symmetrical. If the separate DC-sources for each H-bridge are equal in voltage magnitude it's called symmetrical H-bridge is shown in Fig. 1. If the voltage sources differ in magnitude, it's called asymmetrical H-bridge. Cascaded multilevel inverter has power applications in shunt L series connected facts controllers.

In this topology, there are 2 unequal DC sources and 2 H-bridges, each connected to a DC-Source. By suitable opening and closing of switches of the first H-bridge, the output voltage v1 can be made equal to $V_{DC}$ or+$V_{DC}$ and for the second H-bridge the output voltage can be made equal to -0.5 $V_{DC}$, 0 or 0.5 $V_{DC}$ and the cascaded output is shown having five possible values $V_{DC}$, 0.5 $V_{DC}$, 0, -0.5 $V_{DC}$, -$V_{DC}$ is shown in Fig. 2.

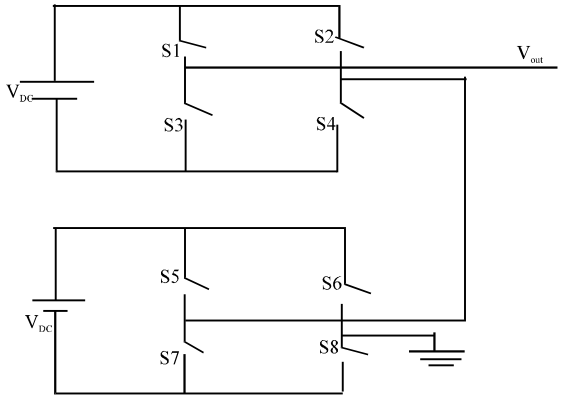


Fig. 1: Structure of a single phase cascaded inverter

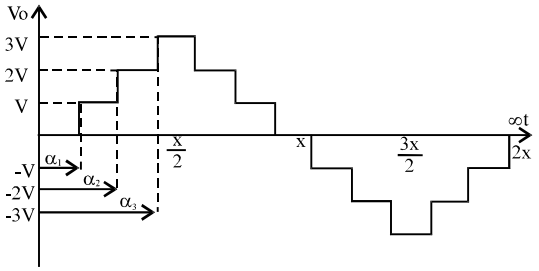


Fig. 2: 5-level stepped output voltage waveform

The conventional 2 or 3 levels inverter does not completely eliminate the unwanted harmonics in the output waveform (Palanisamy *et al*., 2016a, b). So, we go for multilevel inverter where in the final output voltages and is symmetric with respect to neutral point, so, the number of voltage levels is odd (Corzine and Baker, 2002). Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency. The cascaded H-bridge inverter also brought in the concept of Separate DC Source (SDCS) s to produce an AC voltage waveform. The circuit is simulated using MATLAB. IGBT stands for insulated gate bipolar transistor which is a three terminal semiconductor device with the capability to carry high bipolar current. IGBT is accessible for both low switching loss and low conduction loss. Moreover, IGBT has high voltage capability, low on-resistance, ease of drive and relatively fast switching speeds.

### Modes of operation

**Mode 1:** The first mode of operation is when semiconductor switches S1 and S2 are turned on , current starts flowing and we get positive output voltage of 0.5 $V_{dc}$.

**Mode 2:** Both S1 and S3 or S1 and S2 should never be closed at the same time, else it will create a very low resistance path between the power and the ground, thus resulting in short circuit. This condition is called inshoot. Therefore, in mode 2. we switch on switches S2, S3 and then, we get output negative voltage. Here, $V_1 = 0.5\ V_{DC}$; $V_2 = V_{DC}$. The table shows the switching sequence of a cascaded 5-level multil evel inverter.1 indicates on and 0 indicates off. And the total output voltage is $V_{DC} = V_{DC1}+V_{DC2}$.

**Sinusoidal Pulse Width Modulation (SPWM):** Pulse width modulation is a method wherein a fixed DC input voltage is given to inverters and controlled AC output voltage is obtained by adjusting the duty cycle. Output signal alternates between ON and OFF within specified period; controls power received by a device and the voltage seen by the load is directly proportional to the source voltage.pulse width modulation allows us to vary how much time the signal is high in an analog way. While the signal can only be high (usually 5 V) or low (ground) but we can vary the proportion of time the signal is high compared to when it is low is shown in Fig. 3.

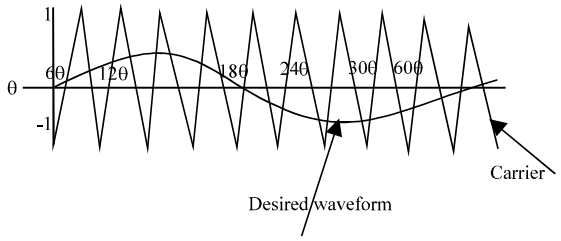


Fig. 3: Sinusoidal Pulse Width Modulation (SPWM)

The main advantage of PWM is that power loss in the switching devices is very low. The technique we are using is the sinusoidal pulse width modulation. SPWM is one of the most popular modulation technique used and finds more applications in industries. The gating signal can be generated by comparing a sinusoidal reference signal with a triangular carrier wave and width of each pulse varied proportionally to amplitude of a sine wave evaluated at the centre of same pulse. SPWM is one technique which helps in reducing the harmonics present in quasi state. The modulation index is defined as:

$$M_a = A_m / A_c$$

Where:

$W_c$ = Reference frequency
$W_m$ = Carrier frequency
$A_m$ = Reference signal amplitude
$A_c$ = Carrier signal amplitude

## RESULTS AND DISCUSSION

The simulation circuit of the proposed cascaded H-bridge five level inverter is shown in Fig. 4. It shows the generated gate pulses using sinusoidal PWM control technique to the multilevel inverter switches. From the

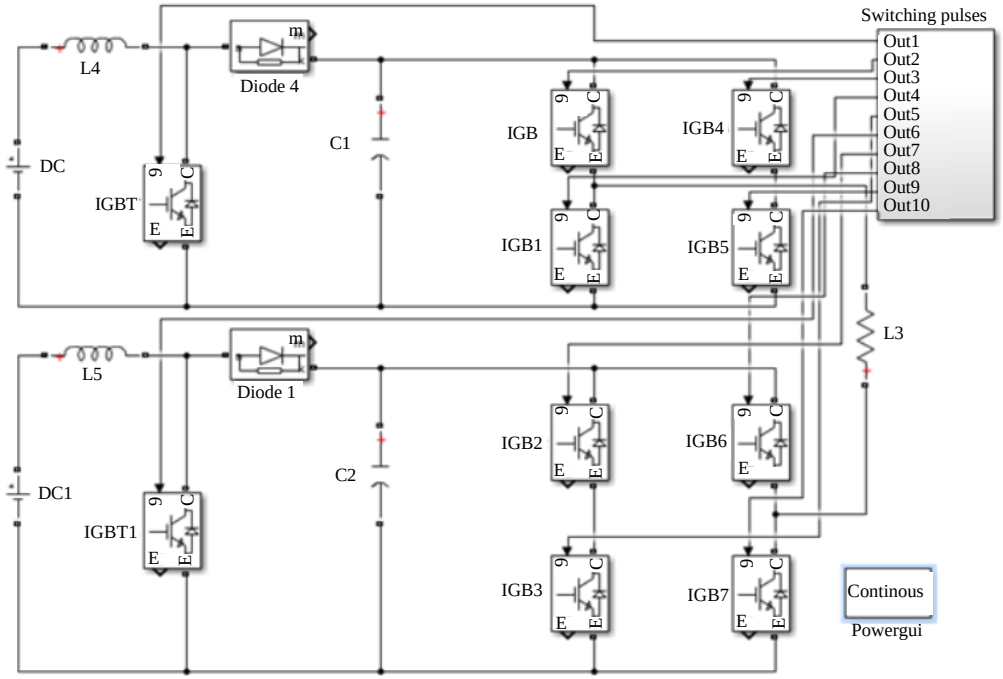


Fig. 4: Simulation circuit of proposed cascaded H-bridge five level inverter

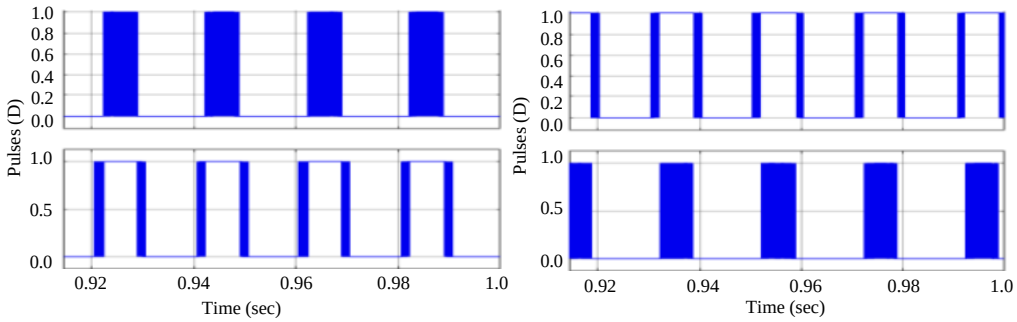


Fig. 5: Gating pulses generation using SPWM scheme

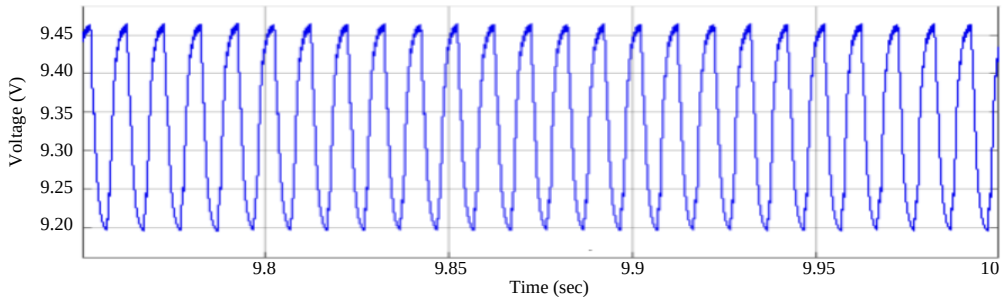


Fig .6: Voltage across switch S1

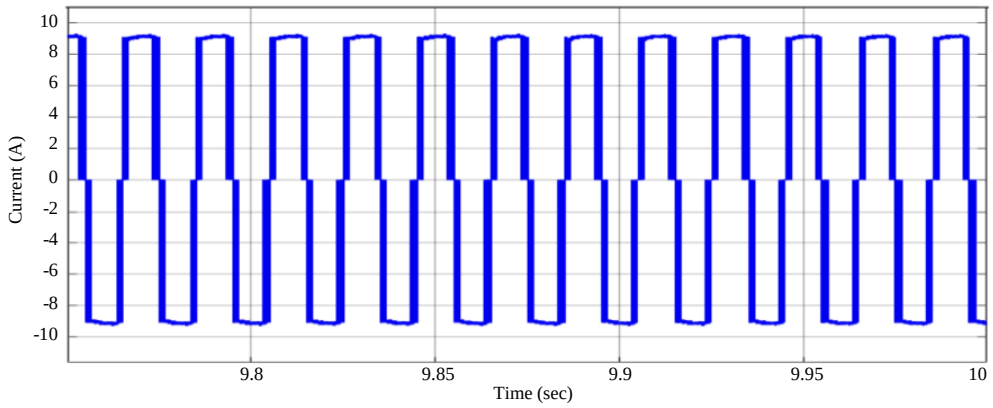


Fig. 7: Output current of 1-phase cascaded H-bridge inverter

gate pulse turn on period it is observed that each switches turned on at different time period to synthesize required output voltage. The proposed circuit needs independent DC source which is supplied from photovoltaic cell or battery or fuel cell. The switching device used is MOSFET. In case of five level inverter requires eight switches to get the five level output voltage. The gating pulses generation using SPWM schemeis shown in Fig. 5 and 6 shows voltage across switch S1. Figure 7 shows output current of 1-phase cascaded H-bridge inverter. The stepped output voltage waveform of 1-phase cascaded h-bridge inverter is shown in Fig. 8. The FFT analysis for five level H-bridge inverter is shown in Fig. 9 and the simulated value of THD is 33.22% which is low when compared to conventional two level inverters (around 60%).

**Hardware:** To authenticate the simulation results of the proposed system, experimental setup 5-level single phase cascaded H-bridge multilevel inverter was designed and tested. Figure 11 shows 5 level stepped output voltage of 1phase cascaded H-bridge inverter and output current waveform is shown in Fig. 10 and 12 shows the experimental setup for the proposed system.

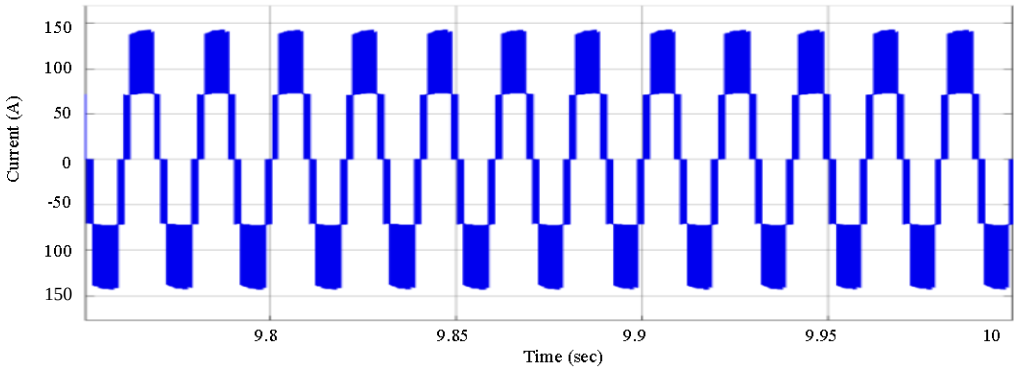


Fig. 8: Stepped output voltage of 1-phase cascaded H-bridge inverter

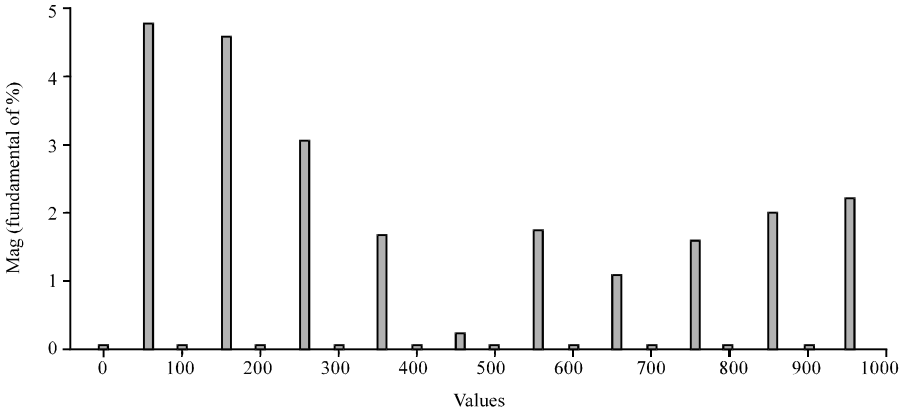


Fig. 9: Harmonic analysis for output voltage of proposed system; Fundamental (50 Hz) = 135.3, THD = 33.22%

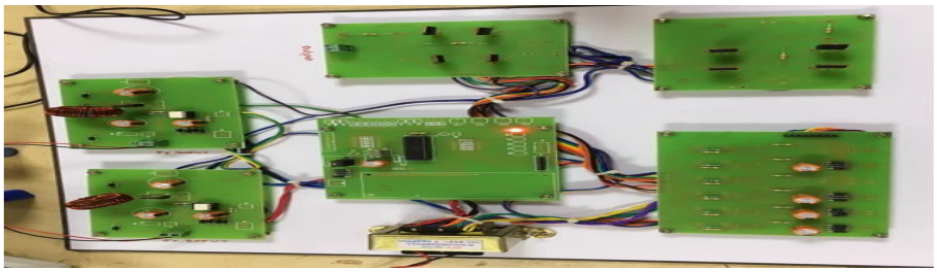

Fig. 10: Experimental setup of proposed system

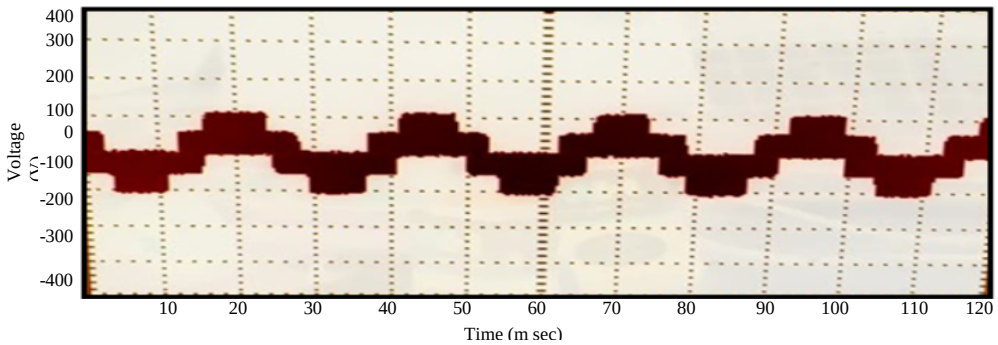


Fig. 11: 5-level output voltage from proposed system

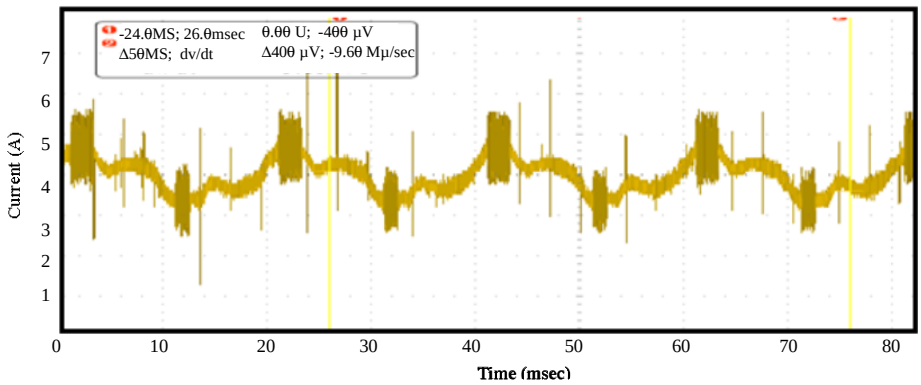


Fig. 12: Output current waveform of proposed system

## CONCLUSION

This study gave idea about 5 levels a five level cascaded H-bridge multilevel with sinusoidal pulse width modulation and MATLAB function is presented. The multilevel inverter consists of two series connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The performance of the five level cascaded H-bridge multilevel inverter employing sinusoidal pulse width modulation technique is found to be superior when compared to the two level inverter. In addition, using sophisticated modulation methods, CM voltages can be eliminated. They can operate with a lower switching frequency. The simulation results prove that with inverter strategy, the low order harmonics are substantially reduced. A THD analysis has been done. Total harmonic distortion or THD is the summation of all harmonic components of the voltage or current waveform.

## REFERENCES

Corzine, K.A. and J.R. Baker, 2002. Reduced-parts-count multilevel rectifiers. IEEE. Trans. Ind. Electron., 49: 766-774.

Corzine, K.A., M.W. Wielebski, F.Z. Peng and J.Wang, 2004. Control of cascaded multilevel inverters. IEEE Trans. Power Electron., 19: 732-738.

Haw, L.K., M.S. Dahidah and H.A. Almurib, 2015. A new reactive current reference algorithm for the STATCOM system based on cascaded multilevel inverters. IEEE. Trans. Power Electron., 30: 3577-3588.

Kouro, S., P. Lezana, M. Angulo and J. Rodriguez, 2008. Multicarrier PWM with DC-link ripple feedforward compensation for multilevel inverters. IEEE. Trans. Power Electron., 23: 52-59.

Lee, J.S., U.M. Choi and K.B. Lee, 2015. Comparison of tolerance controls for open-switch fault in a grid-connected T-type rectifier. IEEE. Trans. Power Electron., 30: 5810-5820.

Manjrekar, M.D., P.K. Steimer and T.A. Lipo, 2000. Hybrid multilevel power conversion system: A competitive solution for high-power applications. IEEE. Trans. Ind. Appl., 36: 834-841.

Palanisamy, R., A.U. Mutawakkil and K. Vijayakumar, 2016a. Hysteresis SVM for coupled inductor Z source diode clamped 3-level inverter based grid connected PV system. Intl. J. Power Electron. Drive Syst., 7: 1181-1192.

Palanisamy, R., K. Vijayakumar, K. Selvakumar, D. Karthikeyan and G. Santhoshkumar, 2016b. Simulation and modelling of 5-level single phase Z-source based cascaded inverter. Indian J. Sci. Technol., Vol. 9, 10.17485/ijst/2016/v9i43/101859

Palanisamy, R., K. Vijayakumar, S. Misra, K. Selvakumar and D. Karthikeyan, 2015. A closed loop current control of PV-wind hybrid source fed on grid connected transformerless diode clamped-multi level inverter. Intl. Rev. Modell. Simul., 8: 386-398.

Peng, F.Z., 2000. A generalized multilevel inverter topology with self voltage balancing. Proceedings of the IEEE 2000 International Conference on Industry Applications Record Vol. 3, October 8-12, 2000, IEEE, Rome, Italy, ISBN:0-7803-6401-5, pp: 2024-2031.

Thongprasri, P., 2011. A 5-level three-phase cascaded hybrid multilevel inverter. Int. J. Comput. Electr. Eng., 3: 789-794.