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Critical Challenges and Solutions for Device Miniaturization in Integrated Circuit Packaging Technology

A.R.A. Rahman and Nazrul Anuar Nayan
Centre for Integrated Systems Engineering and Advanced Technologies,
Faculty of Engineering and Built Environment, University Kebangsaan Malaysia (UKM),
43600 Bangi, Selangor, Malaysia

Abstract: Recently, the number of wearable devices increases due to demands. Therefore, a considerably light, thin and high complexity Integrated Circuit (IC) packaging is desirable. However, several critical challenges exist in implementing ICs in the packaging manufacturing industry. Die cracking and warpage due to high stress are the common failures. These conditions will worsen when using small and thin dies. Package stresses are predominantly caused by the mismatch in the thermal expansion coefficients of the involved materials. This study conducts experimental studies on the critical packaging processes such as backgrinding, wafer sawing, die attachment and wire bonding, using 18×14 mil die size. The manufacturing process stability is developed by process optimization, monitoring and control. Several critical challenges and proposals for device miniaturization in IC packaging are highlighted in conclusion section.

Key words: Packaging, manufacturing industry, backgrinding, wafer sawing, die attachment, wire bonding

INTRODUCTION

In the current electronic world, the number of wearable devices such as augmented reality headsets, smart watches and therapeutic gadgets, increases. Thus, a considerably small, thin, light, highly functional, fast, relatively complex and low-power consumption Integrated Circuit (IC) is desirable. Miniature IC can be converted into small ones in x- and y-sizes and low thickness. Small die is defined as the die with the size of <20×20 mil. However, the challenge is to manufacture a relatively small die but with similar or improved integrated functions added (Zhang *et al*., 2014). Whether the current packaging technology can handle relatively small and thin dies is unknown. Studies should focus on reliability and cost. The semiconductor industry players are expecting low material cost and short lead time at specified quality standards and reliability by transitioning to miniaturization. They introduced new wafer types and silicon technologies. For example, the shift from the use of normal aluminum bond pad to protruded copper bond pad over the circuit of the wafer has remarkably saved 22% of the die size. The new Si technology can shrink the die size by approximately 30% in each generation.

Furthermore, quality issues may arise due to the complexity of the manufacturing process of miniature IC devices. The challenges encountered by the IC packaging manufacturing industry are due to the lack of knowledge and experience in handling small dies. Si is brittle and it may not be able to sustain the stress, thereby causing weak points that lead to die cracking. Cracking may not occur immediately during the process but it can propagate throughout the process or application. Therefore, understanding and following the correct steps are considerably important in dealing with thin and small dies. Stresses in a package are predominantly due to the mismatch of the Coefficient of Thermal Expansion (CTE) of the involved materials (Mokhtar *et al*., 2008) (Maus *et al*., 2017). This condition may worsen because small and thin dies are prone to high stress. In semiconductor plastic packages, moisture can be absorbed through the cracks formed after the CTE mismatch among the lead frame, die and mold (Ng, 2017). Low CTE mismatch between the die attach material and the lead frame will reduce the overall package warpage, consequently, the delamination between these two interfaces is minimized or eliminated (Wai *et al*., 2012).

The key areas identified as critical manufacturing processes are backgrinding, wafer sawing, die attachment and wire bonding. One of the challenges for thin wafers in die bonding process is the die warpage during pickup

Corresponding Author: Nazrul Anuar Nayan, Centre for Integrated Systems Engineering and Advanced Technologies, Faculty of Engineering and Built Environment, University Kebangsaan Malaysia (UKM), 43600 Bangi, Selangor, Malaysia

from the vacuum suction force because thin wafer is largely flexible which may possibly change the profile shape with the changes in vacuum force (Abdullah *et al*., 2012). The need to produce lightweight devices has been the primary reason for the development of thin semiconductor packages (Rasiah and Breach, 2000). During high-speed wafer sawing process, poorly adhered die will fly off, chip or even crack (Tan *et al*., 2015). A small die also indicates a reduction in pad pitch due to the reduced die length (Chong and Tan, 2012). Dispensing pattern is important for die attachment process, complete die area coverage can be achieved with a proper dispensing pattern (Yee and Yew, 2012). Interfaces among electronic packaging materials or components exert a remarkable effect on the thermal impedance of electronic systems and they can be the dominant factors in achieving an effective thermal transfer (Ras *et al*., 2014). Hence, optimization technique helps to identify the best manufacturing parameters (Bachok *et al*., 2008). Some numerical analysis have been done to predict deflection behavior of IC packaging (Hamzah *et al*., 2004; Abdullah *et al*., 2008).

Therefore, solutions on handling small and thin dies in semiconductor packaging should be determined. In the present study, the observed challenges and the proposed solutions for packaging with 18×14 mil die size are presented. For a revision, 1 mil should be 1/1000 inch. Several special solutions for post backgrinding, wafer sawing, die attachment and wire sawing processes are highlighted. Different methodologies are used to deal with small and thin dies. The methodology is developed by considering the risks, quality issues and productivities. A survey on the preference of users on wearable electronic products is conducted prior to this study to understand the market driven by such products. In addition, online surveys are carried out to obtain fast response and a large number of respondents.

MATERIALS AND METHODS

A survey study with 162 respondents is conducted via. LinkedIn to identify the most used electronic products. The questions are related to the electronic products that they currently possess and the sizes, thicknesses, weights, performances and functions they want in products. Subsequently, experimental studies are carried out to identify the critical processes in manufacturing miniature IC packaging and determine solutions. This study uses 18×14 mil die size as shown in Fig. 1. The evaluated IC assembly processes include backgrinding, wafer sawing, die attachment and wire bonding.

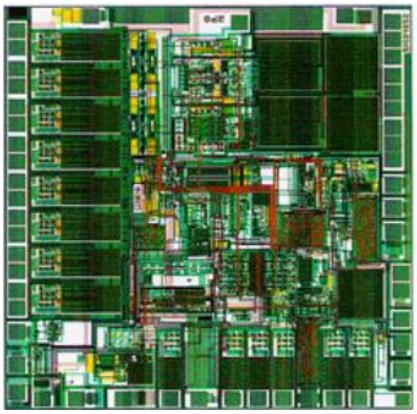

Fig. 1: 18×14 mil die size used in this experimental study

RESULTS AND DISCUSSION

Survey: The participants indicated that hand phone, laptop and digital camera are the top electronic products that they possess at 98.3, 85.6 and 33.1%, respectively. The other electronic items used include wireless Bluetooth headset, fitness pedometer and smart watch.

According to the survey result, 39.8% of the respondents prefer electronic tools with small sizes and 38.1% of them prefer large-sized ones. Only 2.2% seems not to care about the size. Mixed answers of the respondents indicate that people only prefer devices that they are comfortable with. Small-sized products such as pocket-sized hand phones are relatively easy to carry. Large-sized products, such as laptop are relatively easy to work on due to the large screens and keyboards. Approximately 80.5% of the participants prefer thin products and 16.9% of them indicate no care about the thickness. Only 2.6% of the users want thick electronic equipment and 98.3% of them prefer lightweight electronic device. A total of 98.3% of respondents are seeking for high-performance devices. In addition, 72.9% of the users request for high functionality and 25.4% of them prefer simple functionality.

The survey result shows that the trends and preferences in the market for wearable electronics products are small sizes, wide screens, thinness, lightweight, high performance and multifunctionality. Therefore, products in semiconductor manufacturing should require certain key processes to adapt miniature die size.

Packaging process

Backgrinding: The challenge starts in backgrinding which is also called the water-thinning process. The normal wafer thickness of about 30 mils will be reduced to

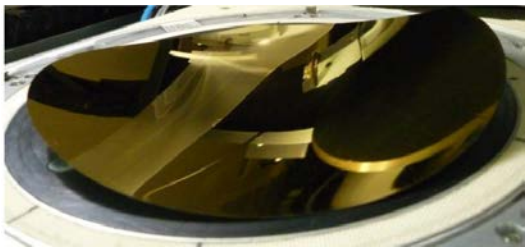

Fig. 2: Warpage on thin wafer

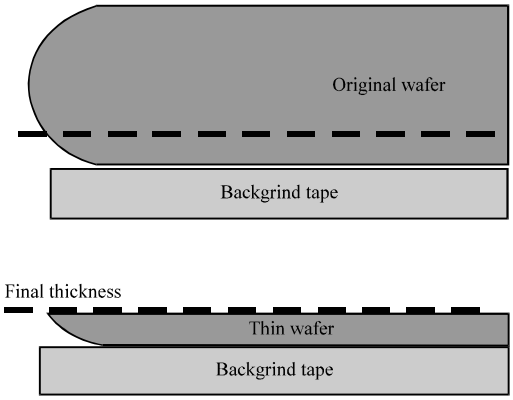

Fig. 3: Sharp wafer edge for thin die

3 mils only. As shown in Fig. 2 with 3 mil thickness, wafer warpage occurs as a result of imbalance stress due to different material layers between the top and back of the wafer. The top surface consists of multiple metal layers and the bottom surface is pure Si. Wafer warpage will affect the wafer sawing process because the vacuum needs support to hold the wafer flat on the chuck table. This condition will also cause side and bottom chippings at the warped portion of the wafer. The warpage will subsequently cause individual die warpage after the sawing process and result in die cracking during attachment. The subsequent challenge in backgrinding process occurs after the completion of fine grinding. The shape of the wafer edge will develop into a knife-tip shape during the detaping process. Thus, this area becomes a highly stressful one as shown in Fig. 3. Backgrinding tape removal can cause the wafer to chip or crack due to the knife-tip shape.

To solve these problems, this study focuses on wafer handling and storage simultaneously to ensure that the thin wafer is unaffected with additional stress. Weak points such as at the side of the wafer are identified. To address the knife-tip shape issue, wafer-edge trimming is performed prior to the backgrinding process to ensure that the stressed area is removed as shown in Fig. 4.

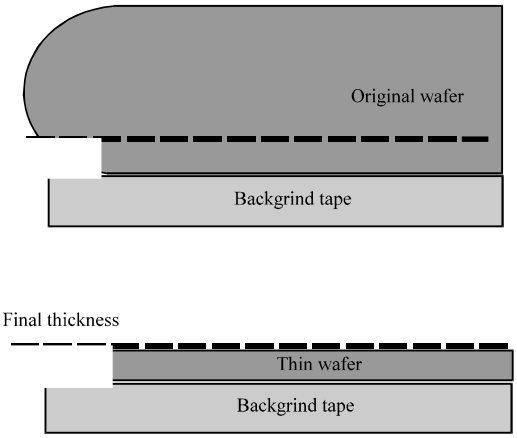

Fig. 4: Thin wafer with trimming edge

Wafer sawing: During the wafer sawing process, the small die encounters problems such as die fly off and bottom and side chippings. The bottom and side chippings are due to the instability of the wafer or its vibration during the sawing process. This phenomenon can be observed during die attachment.

The back of the wafer will be attached to the sawing tape before the process. The wafer sawing process focuses on wafer stability. Bubbles between the mylar tape and the wafer are removed to ensure that all the dies are firmly held during sawing. Consequently, any movement that may cause die chipping can be avoided. Die fly off or neighbor die lifting occurs when the tape adhesion is insufficient to hold the sawn die during the process. Chuck table is used to pull down the entire back surface of the wafer to obtain wafer flatness. Parameter optimization such as feed rate and cutting height for the Z1 and Z2 is also carried out.

Die attach: During die attachment, using small dies may cause die placement and die rotation due to unsuccessful pickup. This deformation may cause vacuum chip sensor error which may lead to false alarm and consequently stop the machine. Therefore, when using small dies, the vacuum hole is also small and the size deformation will affect the pickup force.

Given thin die, the normal die attachment process by using ejector needle may be unsuitable. As depicted in Fig. 5 and 6 an ejectorless system is introduced. This system is consisted of pillars and end support pepperpot, including heater to soften the mylar tape during die pickup. Ejectorless die pickup is used to avoid additional stress to the back of the die. The weak points due to the stress applied will initiate crack which will propagate to the remaining packaging processes, including end-of-line

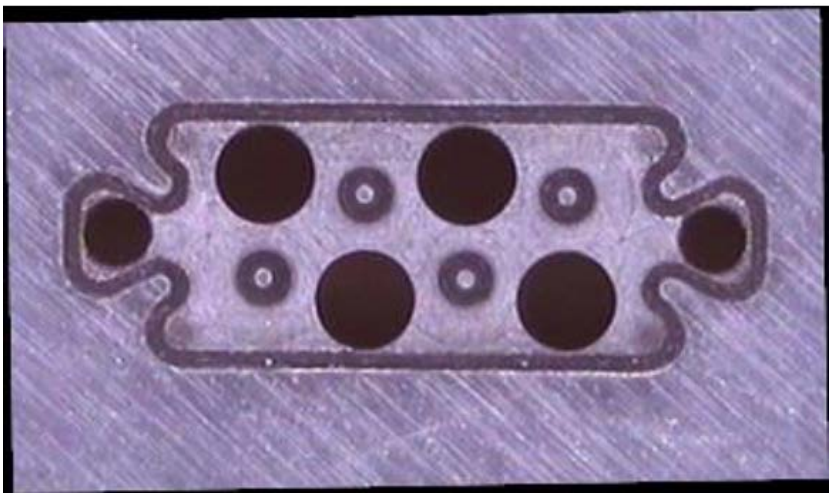

Fig. 5: Ejectorless pickup

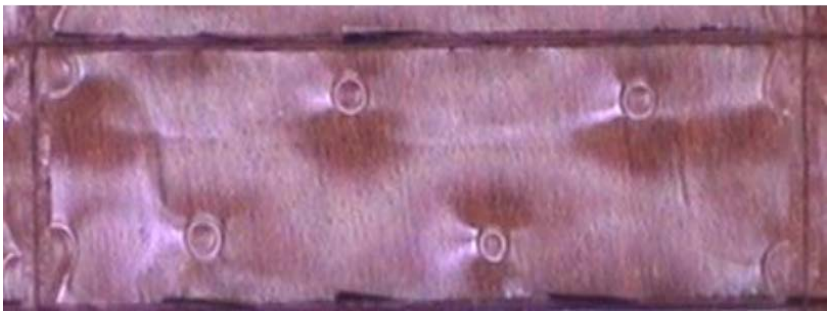

Fig. 6: Imprint of die ejectorless pickup

testing or during application. During die attachment, the focus of the small die pickup is on the pickup mechanism, such as collet and pepperpot. The collet must provide sufficient vacuum suction to pick up the die. The hard rubber or high-temperature rubber collet is used because it shows less deformation during die pickup. Vespel collet causes scratches on the die surface. Furthermore, the pepperpot must possess sufficient vacuum suction to hold the die. The collet surface must present a stopper at the center area to straighten the warpage of the die. The chip sensor detection is critical in determining the die presence and providing signal to the system. The vacuum reading must be consistent to establish the threshold on the existence and nonexistence of the die. As shown in Fig. 7, vacuum reservoir is used to obtain consistent vacuum suction and stable vacuum reading for threshold establishment. The die placement in x- and y-directions and angle are carefully monitored.

The epoxy amount is thoroughly measured to ensure no epoxy tailing issue. The epoxy tailing is due to small epoxy amount and it should be optimized by obtaining the right dispense tip distance to the pad and not causing

Fig. 7: Vacuum reservoir

over gap. Sufficient amount of epoxy under the die and the side epoxy fillet are needed to overcome the warpage movement after the die attachment process. The epoxy pattern should be optimized with additional amount of epoxy to support the center part of the die. The die will move to its equilibrium position of warpage shape after die placement. The additional amount of epoxy at the center will be pulled in under the die which will return to its original warped position. If no epoxy is available then

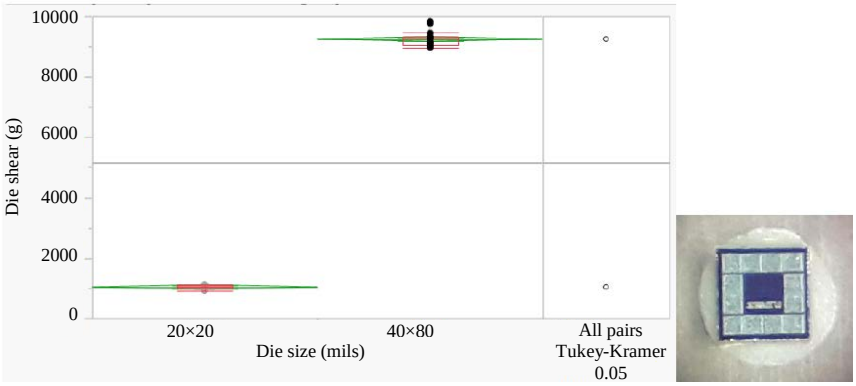

Fig. 8: Die shear test for 20×20 mil vs. 40×80 mil die size (photo)

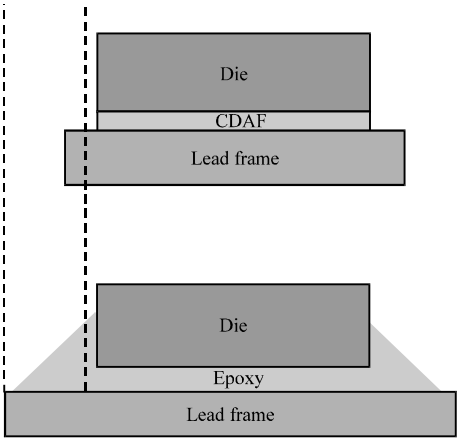

Fig. 9: Space reduction with CDAF

void will occur. Conductive die attach epoxy components include basic resin, hardener, silver filler, coupling agents, solvent and catalyst (Wang and Yeo, 2012).

As shown in Fig. 8, the average die size is 20×20 mil with the weight of 1037.2 g. The common die size is 40×80 mil with the average weight of 9246.5 g. The weight limit of a die with the size of 20×20 mil is 160 g. In this study, the Conductive Die Attach Film (CDAF) is used. The advantage of using the DAF is to acquire small package without the allocation space for the epoxy fillet wet out as demonstrated in Fig. 9. The DAF is the most ideal solution to sustain BaseLine Thickness (BLT) and reduce tilted die issues, delamination and collet contamination due to insufficient curing (Krishnan *et al*., 2014). Tilted die is a common phenomenon that generally worsens the reliability and performance of devices (Zheng *et al*., 2014). Through characterization, the cause of chipping and cracking was evaluated to help in exploring a sawing method to reduce chipping on wafer laminated with conductive DAF (Jiun *et al*., 2006).

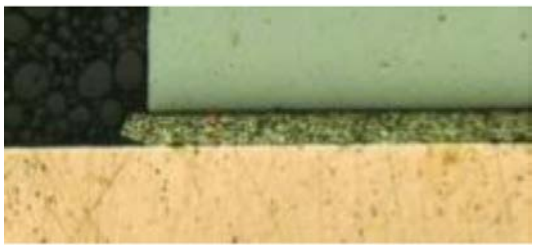

Fig. 10: Two percent void on normal leadframe

The development of DAF is actively considered to replace the typical epoxy process. As shown in Fig. 10, good results with 2% total void issue are achieved. The largest void percentage instead of the total void percentage considerably affects the thermal dissipation of devices (Singh *et al*., 2017). The parameters are optimized using scrub cycle with long effective time. The CDAF requires bonding delay and high temperature to allow the file to melt, solidify and stick to the lead frame (Jalar *et al*., 2008).

Wire bonding: Issues encountered during the process are as follows: NonStick On Pad (NSOP), lifted ball during pull test and low ball reading during shear test. The wire bond interconnection may be affected with delamination which causes the separation between the ball and the bond pad. Another challenge with the miniature die is that the metal protrudes on its top as shown in Fig. 11. This condition will lead to high stress and cause the delamination on the top of the die and the possible functionality and reliability issues.

In wire bonding process, surfactant is used to prevent any galvanic corrosion or dust accumulation, especially on the bond pad area. Copper wire size reduction indicates that the small bond pad size should be used. The first wire bond should be characterized. This process is performed to evaluate the sensitive brittle

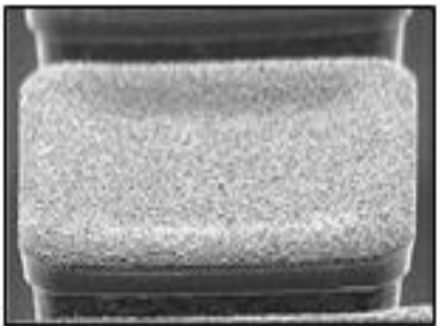

Fig. 11: Cu protruded bond pad

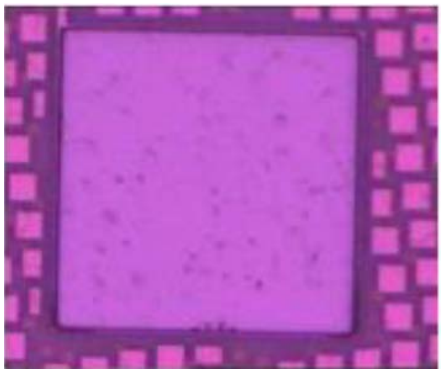

Fig. 12: Flat Cu bond pad

material used and metal stack differences during die size reduction. Using Cu wire instead of Au wire becomes relatively challenging due to the difference in hardness. Several customized bond pad types have been used as options. Other important wire bond parameters such as UltraSonic Generator (USG), bond force and bond time, should be evaluated during the design of experiment after the first bond. The optimization factors when using customized designs are USG, time, force, initial force scrub and scrub cycles. The results are NSOP, metal peeling during bonding, ball shear, wire pull, lifted metal during wire pull, lifted ball during wire pull, lifted metal during ball shear and lifted ball during ball shear. According to the statistical tool software contour profiler, the safe region based on the desired results is selected. The region is targeted to be at the center of the parameters. The optimized parameter is tested with confirmation run to validate the results with no issue. In the present study, the 0.96 mil gold wire is replaced with 0.8 mil copper wire which is small to fit into the small bond pad but maintain the same robustness. This replacement will satisfy the design requirement that 5 μm per side spacing should be ensured between the edge of the wire ball and the edge of the bond pad.

To eliminate bond pad protrusion, CuNiPd as the top metal is used in this study as shown in Fig. 12. The metal

Fig. 13: Bond on high thickness Al bond pad

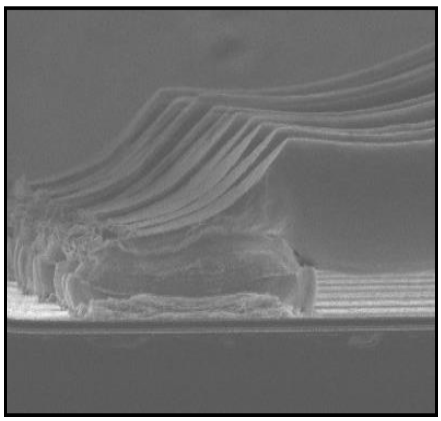

Fig. 14: Stand off Stitch Bond (SSB)

thickness may be different in terms of compatibility to the wire bonding process and it works well. Another benefit is the improved die surface stress relief due to the flat and smooth structure of the bond pad on the die. The Cu layer thickness is approximately 3 microns. A tantalum nitride barrier metal covers at the side of the bond pad. Additionally, the cost advantage lowers the amount of the material used and processing method.

With regard to the aluminum bond pad, aluminum splash is observed around the ball in the direction of the ultrasonic movement, as demonstrated in Fig. 13. The aluminum splash will cover approximately 3 microns. Therefore, this splash becomes a disadvantage in obtaining small bond pad and small die size. In addition to a thin die, wire loop is also part of the semiconductor packaging. Low loop is suitable and it can be implemented by using a Stand-off Stitch Bonding (SSB) on the wire bond (Fig. 14). SSB can also be used for die bonding. Reverse bonding is used from the lead to the bond pad.

The miniaturization of the IC packaging as a customer and user requirement is considerably important in semiconductor packaging. Using small and thin die and

package results in lightweight devices. Many commercial devices such as wearable products, need such technology.

Developing small devices is achievable with the introduction of Si nodes which can also save Si usage. The use of different materials by attaching the conductive die film to replace epoxy may minimize epoxy fillet wet out. A process should be developed for small dies and package to ensure manufacturability. The processing time for the small die with 300 mm wafer will be long. The bond pad quality must be high and free from any corrosion. Thus, surfactant usage may be considered.

Thin devices can be produced through backgrinding, sawing and die attachment. The edge trimming prior to the backgrinding process can address the wafer chipping or cracking. Process optimization during die attachment process using ejectorless pickup will ensure no crack in the die. Proper handling should also be considered to avoid package warpage.

Die attachment must be redesigned to equip small die by considering the sensitivity of die placement. Collet size and optimized parameters are needed. Wire bonding must use the optimized capillary and evaluated parameters. The Cu wire can be used for small bond pad die with conductivity of 30% higher than that of the gold wire.

The SSB is used in wire bonding to achieve low loop and determine the mold cap with low dimension. The stress on the die paddle should be avoided along the end-of-line process and evaluated because it may cause hairline cracking on the die. The package design and material selection should be carefully carried out to minimize the warpage which may cause stress to the die.

CONCLUSION

A number of experiments with solutions are performed in manufacturing plants to develop miniature IC packaging and simultaneously maintain the same functionality.

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