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Effect of Threshold Roll-Off on Static Noise Margin of Sram Cell

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Abstract: The threshold roll-off is a vital phenomena to be considered for any low-power and small-scale circuit design. With the advancement of the fabrication processes the channel length of the transistors is reducing rapidly, this reduction in the channel length affects the threshold voltage of the transistors very severely. To evaluate the effect of channel reduction on the threshold voltage this study analyzes the threshold roll-off by taking SRAM cell into consideration. The reason behind choosing SRAM cell is that now the IC's are fabricated using System on Chip (SOC) design technique and currently approximately 70-80% of the SOC area are covered by memories only. One of the most important figure of merit for SRAM cell is its Static Noise Margin (SNM) and hence, the effect of threshold-roll is implemented with respect to SNM of the SRAM cell.

Key words: Threshold roll-off, sub-threshold current, SRAM cell, System on Chip (SOC), Static Noise Margin (SNM), phenomena, transistors

INTRODUCTION

In the current digital integrated circuit designing a complete system is being implemented on the chip which is formally known as System on Chip (SOC). Nowaday, the designed SOCs usually contain memory in its larger part of the area (roughly 70-80% of its total area), Hence, it is very crucial to take the memory part in a very effective way as the memory cells are very compact compared to other logic parts present in the chip. The care should be taken in such a manner that even if a single cell is defective then it must be identified otherwise it may affect the adjacent cell and may damage the functionality of the whole memory component (Zhang *et al*., 2010; Shih *et al*., 2005; Lundstrom, 2003; Chang *et al*., 2003; Ito *et al*., 2003; Zhao and Cao, 2006; Ishii *et al*., 1998; Shee *et al*., 2014; Austin *et al*., 1998).

However, as the fabrication process of the integrated circuits are advancing quickly, it affects the size of the transistors or other components present in that chip. Presently many vendors are working on <20 nm process technology which directly has impact on the size of transistors short channel length is one of the impacts of this scaling. Due to continuous scaling of the various parameters the threshold roll-off comes in the design issue and this issue may affect the behavior of the component or the entire system very badly.

An SRAM cell is taken in this case to analyze the effect of threshold roll-off on its static noise margin as the SNM of the SRAM cell is very crucial design issue for the cell stability and how effectively an SRAM cell can read and/or write is determined by its SNM analysis only. If the SNM of the cell is not properly optimized it may degrade overall functionality of the entire memory of the IC.

MATERALS AND METHODS

Threshold roll-off: According to the classical theory of the transistors in the channel region for depletion charges the gate voltage has to be compensated before making the channel to go into strong inversion. This gate voltage is responsible for the constitution of the threshold voltage given in Eq. 1:

$$V_T = V_{FB} + 2\varphi_F + \frac{\sqrt{2\varepsilon_0\varepsilon_{si}\, qNA}}{C_{ox}}\sqrt{2\varphi F} \quad (1)$$

Where:
VFB = The Flat Band Voltage
NA = Accepter concentration
φ = F Fermi level

However, a very small amount of the depletion charges caused by the source and drain junction present near the source and drain region, this in turn increases the leakage current. For long channel transistors, this effect is negligible while comparing to the overall depletion

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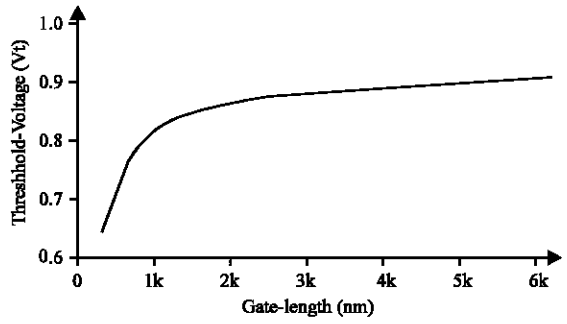

Fig. 1: Threshold roll-off w.r.t gate length

Table 1: Geometric parameters

Gate length (nm)	16 nm	22 nm	32 nm	45 nm
Dielectric thickness	1.2e-9	1.4e-9	1.6e-9	1.8e-9
Junction depth	5e-9 7	2 e-9	5e-8	1.4e-8
Channel depletion thickness	5e-9	7.2 e-9	5e-8	1.4e-8

Table 2: Parameters

Gate length (nm)	16 nm	22 nm	32 nm	45 nm
EI	1.00055	1.04	1.0061	1.0000154
VT-roll	1.886 φD	1.963 φD	1.899 φD	1.888 φD

charges. This effect comes into the design where transistor channel length or gate length is short as shown in Fig.1.

The other factors which affect the threshold roll-off include gate-oxide thickness, channel-depletion depth and junction-depth as the length of the channel becomes shorter. By optimizing inner junction and depletion depth, the threshold roll-off may be controlled till a certain extent. Another most critical effect is charge sharing in short channel transistors. Empirically, the Threshold roll-off approximately calculated is given by Eq. 2:

$$V_T = 0.64(\varepsilon_{si}/\varepsilon_{ox})(\varphi_D)(EI) \quad (2)$$

where, φ_D D is source to channel junction built in voltage and EI is known as electrostatic integrity of the device and calculated using:

$$EI = 1+\frac{xj^2}{L^2}.\frac{t_{ox}}{L}.\frac{T_{dept}}{L} \quad (3)$$

where, T_{depl} is the depletion depth in the channel. Hence, from above equation, we can conclude that by reducing the value of EI in the device structure the threshold roll-off voltage can be reduced. The modeling for transistors is related to its device geometric parameters as shown in Table 1.

The calculated values of EI and VT-roll are shown in Table 2. From this expression, it is also clear that the threshold roll-off depend largely on source to channel

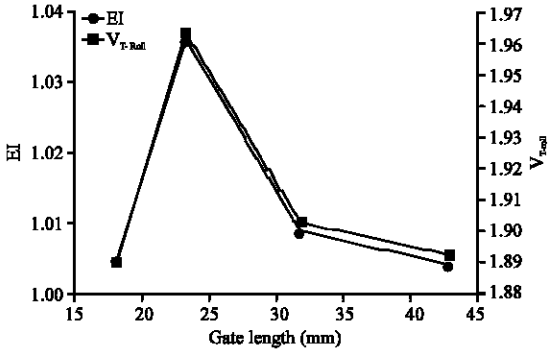

Fig. 2: Variation of $V_{T\text{-}Roll}$ and El w.r.t gate length

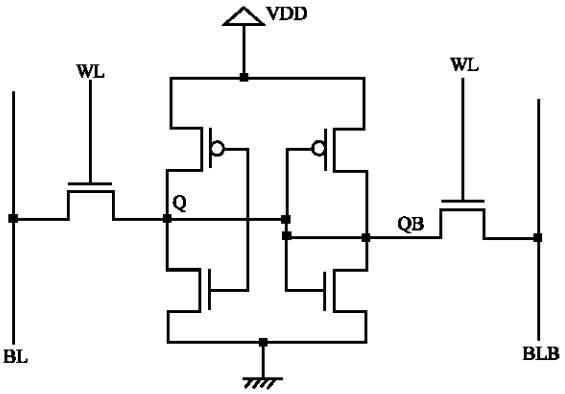

Fig. 3: Basic single port SRAM cell

built-in voltage (φ D) rather than electrostatic integrity only (if EI is somehow maintained nearly equal to 1 as it is always desired).

The source to channel built-in voltage (φ D) can be calculated using in Eq. 4 and by varying the involved parameters the VT-Roll can be controlled as per the requirements:

$$\varphi_D = V_{tm} * \ln(SD*N_D/n_i^2) \quad (4)$$

Where:

SD = Substrate Doping

N_D = Donor density

n_i = Intrinsic carrier concentration

The final graph is plotted between gate length, EI and $V_{T\text{-}Roll}$ as shown in Fig. 2. By observing the obtained graph it can be concluded that the variation is almost constant w.r.t. EI as well as φ D. Hence, the $V_{T\text{-}Roll}$ is not only dependent on EI but also it depends on the value of φ D and by controlling the value of it the $V_{T\text{-}Roll}$ can also be controlled.

Sram cell: The basic single port SRAM cell is shown in Fig. 3. It consists of two inverters connected back to back

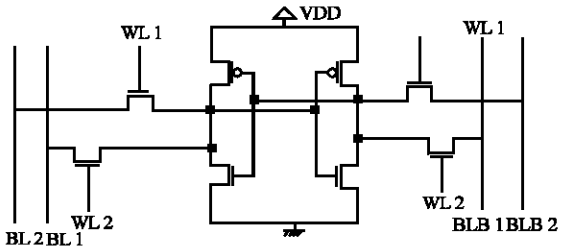

Fig. 4: Double port SRAM cell

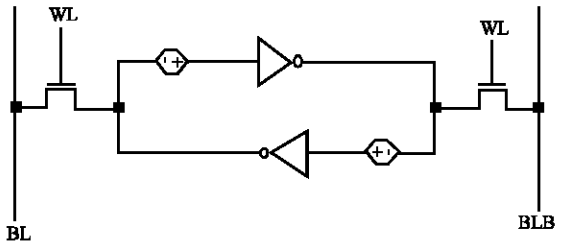

Fig. 5: Arrangements of SRAM cell for measuring its SNM

and this connection is responsible for the reinforcing the cell and make it suitable for data retention. The Bit-Lines (BL and BLB) are used for reading and writing the data from the memory while the Word Line (WL) is used for selecting the particular cell of the memory.

The above cell is just a single read/write cell, however now most of the memories contain double or dual port read/write cell as shown in Fig. 4. Double port SRAM cell increases the memory density to a higher extent.

The two ports present in the given cell is able to access the cell independent to each other but to achieve this the bit lines (also known as access lines) and word lines should be duplicated. In the above cell, two extra pass transistors are required to control the access of the second port (Inaba *et al*., 2002; Khakifirooz and Antoniadis 2006; Abd-Elhamid *et al*., 2006; Pavlov and Sachdev, 2008; Farkhani *et al*., 2014) (Table 3).

Static noise margin: For SRAM cell, its SNM is a key figure of merit. The SNM can be calculated by drawing a largest possible square in between the two Voltage Transfer Characteristics (VTC) of the back to back connected inverters the configuration can be shown in Fig. 5.

Where the voltage source is given as noise voltage source. The side length of the square which is usually given in volts represents the SNM of the cell. When the given noise voltage is increased and becomes more than SNM, the state of the SRAM cell may alter and the data may lost which is not a desired result. Furthermore, since

Table 3: Parameters

Device name	Mos size W/L (nm)
PMOS	200/70
NMOS	66/22
Supply voltages (V)	
V_{DD}	3.8
Word Line (WL)	1.6
Bit Line (BL)	1.6

the cell perform both read as well as write operation of the data the SNM also characterized as read as well as write margin. In the case of read margin the SNM is calculated when the word line voltage is set high and the bit lines are also recharged to its high value on the other hand the write SNM is defined as the minimum bit-line voltage required to change the stored data of the cell.

RESULTS AND DISCUSSION

The above single and double port SRAM cell is simulated using HSPICE simulator and their threshold roll-off is maintained by varying the device parameters as shown in Eq. 2 and 3. The noise margin simulation is also performed to measure the effective SNM of both the cell with respect to the optimized threshold roll-off. The standard 22 nm process technology is used for the modeling of transistors. The various other major parameters are noted in Table 3.

Figure 6a shows the value of supply voltage is given to VDD and WL port of the cell. In Fig. 6b, the bit line signal is shown, However, the output can be observed by Fig. 6c which shows the value at Q and QB node of the SRAM cell.

Now, Fig. 7a, b shows the voltage transfer characteristics of the inverters used in the SRAM cell design. As it can be clearly seen from Fig. 7b that how the threshold roll-off affects the VTC of the inverter and this further influence the SNM of the cell (Hassanzadeh *et al*., 2013; Dhilleswararao *et al*., 2014; Wang, 2011; Madiwalar and Kariyappa, 2013; Sil *et al*., 2008; Sil *et al*., 2007; Wang and Choi, 2011; Nii *et al*., 2004; Premalatha *et al*., 2015; Wong, 2011).

Figure 7 and 8a, b show the static noise margin of the single port and double port SRAM cell respectively. This is obtained by taking the VTC curve of the inverter connected back to back as shown in Fig. 5. The square drawn in between the two VTC will be used for calculating the SMN value in volts.

Since, the design is working under the optimized threshold roll-off condition, so, it is necessary to check the current flow through the circuit. Figures 9a, b represent the current flow w.r.t. the supply voltage for single and double port SRAM cell, respectively. Now finally, Table 4 can summarize the obtained results of the two cells w.r.t. threshold roll-off.

Table 4: Parameters

Single SRAM cell		Double SRAM cell	
Variables	Values	Variables	Values
Read margin	340 mV	Read margin	310 mV
Write margin	290 mV	Write margin	250 mV
SNM	380 mV	SNM	320 mV
Current (max.)	≈110 μW	Current (max.)	≈260 μ W

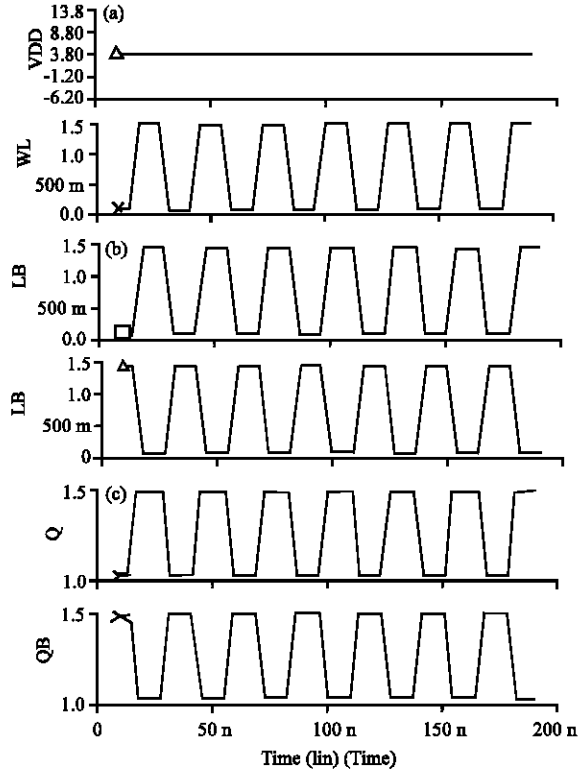

Fig. 6: Values of super voltage

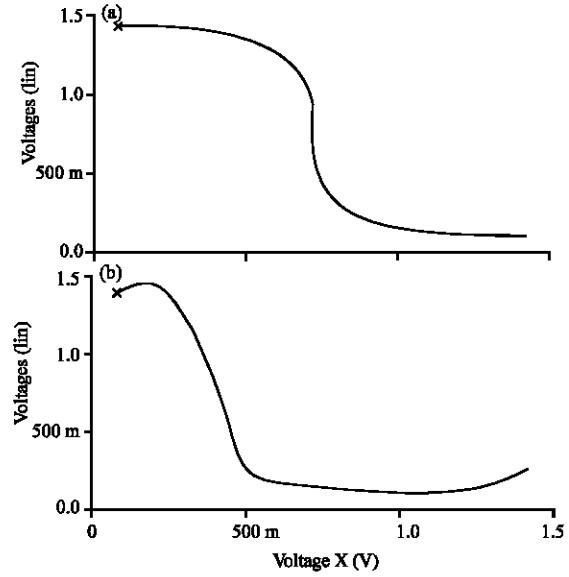

Fig. 7: Voltage transfer charecterstics

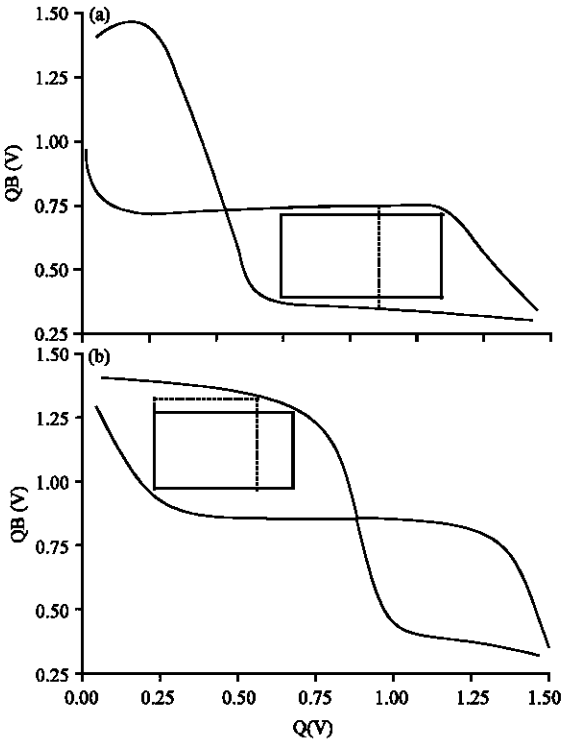

Fig. 8: Static noise margin

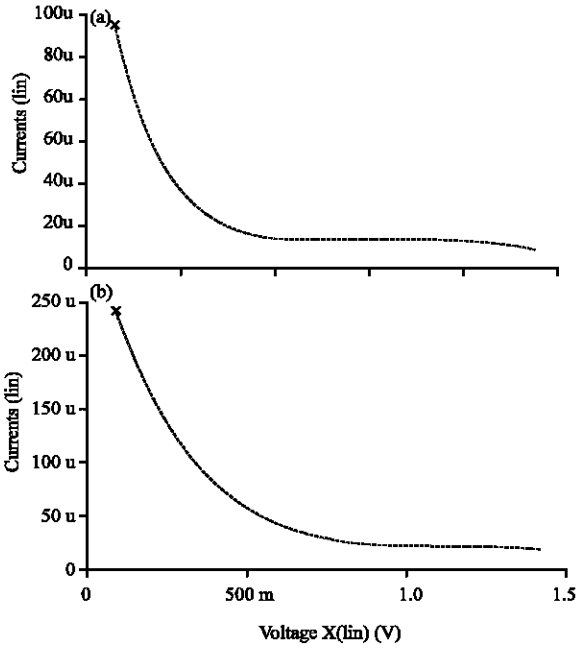

Fig. 9: Current flow

CONCLUSION

This study presents the static noise margin analysis of two different SRAM cell by optimizing the threshold

roll-off of the MOS device used in the cells. The threshold roll-off directly affects the sub-threshold current of the device which inturn affects the device performance in our case the SNM of the SRAM cell is chosen, since, the SNM of the cell is a key parameter design issue for stability and data retention of the cell. If the SNM is low the data which is stored into the cell may lost quickly and our memory may not work as desired. Hence, the device parameters are optimized and that the obtained SNM of the cell is suitable for memory cell design and proper data retention application.

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