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A 31-Level Asymmetrical Cascaded H Bridge Multilevel Inverter

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Abstract: This project commenced with a 31-level Asymmetrical Cascaded H-Bridge Multilevel Inverter (ASCHBMLI). The topology is based on a cascaded connection of single stage sub multilevel converter unit and full bridge cascaded H-bridge inverter. The input DC voltage source of V_{dc1}-V_{dc4} are planned in paired type of voltage of 15 V_{dc1}, 30 V_{dc2}, 60 V_{dc3} and 120 V_{dc4} individually. The output voltage levels are 2*(1+2+4+8)+1 = 31) 31 level. The low frequency pulse width modulation technique is utilized for controlling the power semiconductor switches in the ASCHBMLI. Total harmonic distortion is analyses and executed in real time system using PIC16F877A microcontroller.

Key words: The 31 level multilevel inverter, modulation technique and PIC16F877A controller, semiconductor, distortion, output, voltage

INTRODUCTION

Inverter can be comprehensively characterized into single inverter and Multilevel Inverter (MLI). The Multilevel Inverter (MLI) solidify a power semiconductor switches (MOSFET, IGBT, etc., so on), DC voltage source and load (Alamria and Darwish, 2015).

The output voltage of MLI which make the stepped waveforms over the load. In comparison with conventional two level Voltage Source Inverter (VSI), the multilevel inverter which pass on the "n" number of levels interminable supply of switches and DC source. It required for lessening the harmonic distortion and lower electromagnetic interference. On an incredibly essential level there are three sorts MLI, they are named Neutral point Clamped Multilevel Inverter (NPC-MLI), Cascaded H Bridge Multilevel Inverter (CHB-MLI) and Flying Capacitor Multilevel Inverter (FC-MLI) as showed up in Fig. 1.

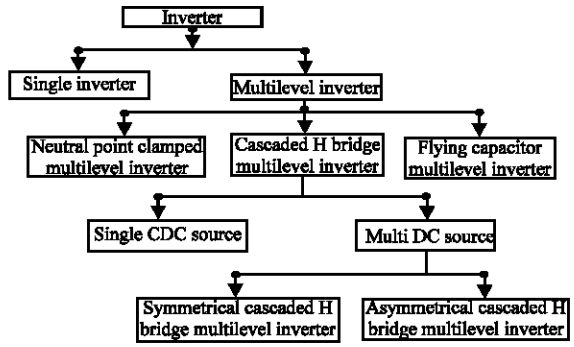

Fig. 1: Classification of multilevel inverter

In MLI, the CHBMLI arrangement draws in more research consideration than FCMLI and NPCMLI because of their circuit simplicity and modularity.The CHB-MLI are named single DC source and multi DC source. In single DC source the CHB-MLI are assocaited in parallel. The ouput voltage of each H bridge, primary side of the transformer is associated where as the secondary side of transformers are related in sereis across the load. In multi DC source the CHB-MLI utilize the arrangement related to each cascaded H-Bridge cells with an isolates DC voltage sources associated with each cell (Paraniya and Sathick, 2016; Lee and Lee, 2013). The CHB multilevel inverters can be divided into two groups from the perspective of estimations of the DC voltage sources: the symmetric and the asymmetrical topology. In the symmetric topology, the DC voltage sources are indistinguishable. If the DC source to SCHBMLI are in the extent that is V_{dc1}-V_{dc4}: is 1:1:1:1. So, the most exterem ouput voltage is (2*(1+1+1+1)+1 = 9) 9 level. In ASCHBMLI is to assemble the measure of output voltage level and the estimations of the DC voltage sources are chosen to parallel, these topologies are called Asymmetrical topology (Naresh *et al*., 2014; Mokhberdoran and Ajami, 2014).

Asymmetrical multilevel inverter: Figure 2 demonstrates the each sub-multilevel inverters are associated in arrangement to accomplish the output voltage and number of levels. The sub-multilevel inverter comprises of DC voltage sources and IGBT switches. In IGBT a portion of the switches are unidirectional and others are bidirectional switches. The unidirectional switches control of Insulated Gate Bipolar Junction Transistor (IGBT) with

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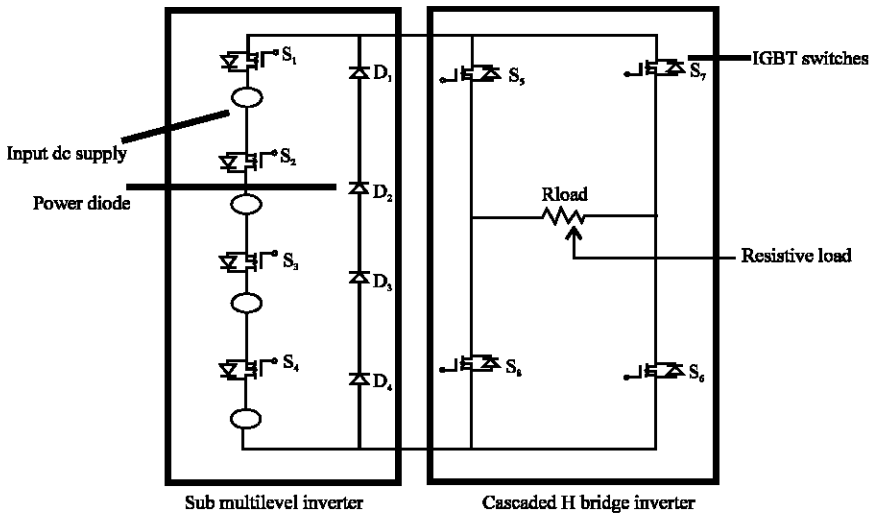

Fig. 2: The 31-level asymmetrical multilevel inverter

an anti-parallel diode. The DC voltage sources of Multilevel inverter are associated in arrangement to get the positive and zero to get the negative from the inverter in each half cycle the cascaded H bridge inverter associated in arrangement with sub multilevel inverters (Atithi and Patel, 2015; Prathiba and Renuga, 2012). The DC source of first, second, third and fourth sub multilevel inverter is V_{dc1}-V_{dc4}:

$$V_{dc2} = (n+1)*V_{dc1} \quad (1)$$

$$V_{dc3} = (n+1)*V_{dc1}+V_{dc2} \quad (2)$$

$$V_{dc1} = (n+1)^{i-1}*V_{dc1} \quad i = 1, 2, 3, ..., m \quad (3)$$

The number of voltage levels will be equal to:

$$N_{level} = 2(n+1)^{m}-1 \quad (4)$$

N = Number of DC input sources
m = Number of sub multilevel in the system

$$N = 2 \text{ and } m = 4 \quad (5)$$

$$N_{level} = 2(4+1)^{4}-1 \quad (6)$$

As per the asymmetrical topology, the estimation of the DC voltage sources is not the same as a submultilevel inverter to another. As such if the DC sources of the main submultilevel inverter is V_{dc1}, the DC source of the second submultilevel inverter is V_{dc2}.To get most extreme number of level for the output voltage, there must be no repetition (Shankar and Edward, 2016). This is accomplished when the estimation of the DC voltage sources in submultilevel inverters have the accompanying connection. Note that the 31-level topology can be given through structure exhibited in Fig. 1 where the main distinction will be in the extremity of the connected DC voltage sources (Rawat and Chandel, 2013).

In ADCS the DC voltage source are in binary form of voltage like 15 V_{dc}, 30 V_{dc}, 60 V_{dc} and 120 V_{dc} So, the output voltage levels are 31 levels. The output voltage levels are 15 V_{dc}, 30 V_{dc}, 45 V_{dc}, 60 V_{dc}, 75 V_{dc}, 90 V_{dc}, 105 V_{dc}, 120 V_{dc}, 135 V_{dc}, 150 V_{dc}, 165 V_{dc}, 180 V_{dc}, 195 V_{dc}, 210 V_{dc}, 225 V_{dc}, 0 V_{dc}, -15 V_{dc}, -30 V_{dc}, -45 V_{dc}, -60 V_{dc}, -75 V_{dc}, -90 V_{dc}, -105 V_{dc}, -120 V_{dc}, -135 V_{dc}, -150 V_{dc}, -165 V_{dc}, -180 V_{dc}, -195 V_{dc}, -210 V_{dc}, -225 V_{dc}. The proposed sub-multilevel inverter can simply create zero and postitive voltage levels. The output voltage is gained when the switchs S_1 and S_1 are turned ON in the mean time. The other voltage levels are created by real trading between the switches. Suggests that the comparing switch is turned ON and 0 shows the OFF stat (Pols and Moring, 2012; Atallah *et al*., 2014) (Table 1).

Switching mode operation of 31-level asymmetrical MLI: The switching technique of 31 level ASCHBMI as shown in Fig. 3 and 4. Conduction plots for switches are controlled by utilizing voltage reference technique. Voltage reference technique changes the switching angles into switching reference voltage. Figure 3 demonstrates the reference voltage waveform with each progression level. Switching reference voltage can be obtained as takes after (Fairchild Semiconductor, 2015). Conduction

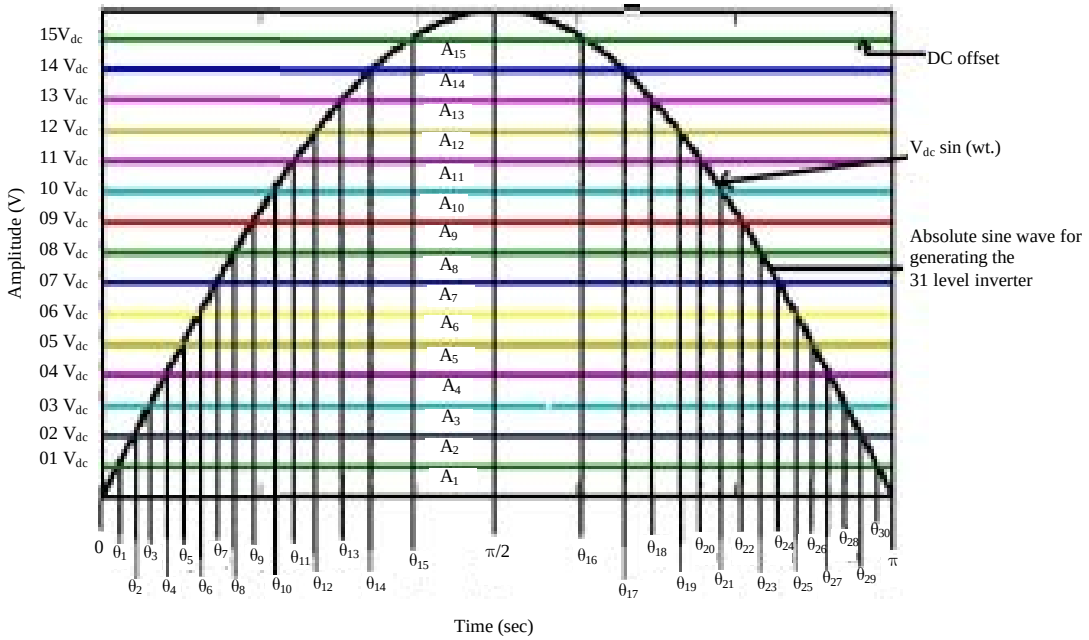

Fig. 3: Reference voltage and step pulse area in 31-level inverter

Table 1: Switching table for asymmetrical multilevel inverter

Factors	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
15 V_{dc}	1	1	1	1	1	1	0	0
14 V_{dc}	0	1	1	1	1	1	0	0
13 V_{dc}	1	0	1	1	1	1	0	0
12 V_{dc}	0	0	0	1	1	1	0	0
11 V_{dc}	1	1	0	0	1	1	0	0
10 V_{dc}	0	1	0	0	1	1	0	0
9 V_{dc}	1	0	1	0	1	1	0	0
8 V_{dc}	0	0	1	0	1	1	0	0
7 V_{dc}	1	1	1	1	1	1	0	0
6 V_{dc}	0	1	0	1	1	1	0	0
5 V_{dc}	1	0	0	1	1	1	0	0
4 V_{dc}	0	0	0	1	1	1	0	0
3 V_{dc}	1	1	1	0	1	1	0	0
2 V_{dc}	0	1	1	0	1	1	0	0
1 V_{dc}	1	0	1	0	1	1	0	0
0 V_{dc}	0	0	0	0	0	0	0	0
-1 V_{dc}	1	0	0	0	0	0	1	1
-2 V_{dc}	0	1	0	1	0	0	1	1
-3 V_{dc}	1	1	0	1	0	0	1	1
-4 V_{dc}	0	0	1	1	0	0	1	1
-5 V_{dc}	1	0	1	1	0	0	1	1
-6 V_{dc}	0	1	1	0	0	0	1	1
-7 V_{dc}	1	1	0	0	0	0	1	1
-8 V_{dc}	0	0	0	0	0	0	1	1
-9 V_{dc}	1	0	0	0	0	0	1	1
-10 V_{dc}	0	1	1	1	0	0	1	1
-11 V_{dc}	1	1	1	1	0	0	1	1
-12 V_{dc}	0	0	1	1	0	0	1	1
-13 V_{dc}	1	0	0	1	0	0	1	1
-14 V_{dc}	0	1	0	0	0	0	1	1
-15 V_{dc}	1	1	0	0	0	0	1	1

plots for switches are controlled by utilizing voltage reference strategy. Voltage reference strategy changes the changing points into exchanging reference voltage. Figure 3 demonstrates the reference voltage waveform with each progression level. Exchanging reference voltage can be gotten as takes after:

$$V_{ref} = m*V_{dc}*M_i*\sin(wt) \quad (7)$$

Where:

m = No. of voltage levels of cascade inverter during one cycle

M_i = Modulation index = V^*/V_{max}

V^* = Amplitude of reference Voltage

V_{max} = Maximum amplitude of cascade inverter

m = 15 and M_I =1 , then $V_{ref} = 15*V_{dc}*\sin(wt)$

Here, reference waveform is isolated into number of ranges which is equivalent to number of ventures in one cycle and the voltage second zone of reference voltage waveform is equivalent to output voltage waveform of inverter. In every range convergence point known as sham edges can be computed by using $\theta_k^1 = \sin^{-1}$ (k/m) where K = 1, 2, 3 (M-1). Then area $A_1, A_2, \ldots, A_J$ can be obtained by using dummy switching angle:

$$A_1 = \int_0^{\theta_1^1} 15V_{dc}\sin(wt)d(wt) + \int_{\theta_1^1}^{\pi/2} V_{dcd}(wt) \quad (8)$$

$$A_2 = \int_0^{\theta_2^1} 15V_{dc}\sin(wt)d(wt) + \int_{\theta_{21}^1}^{\pi/2} V_{dcd}(wt) - A_1 \quad (9)$$

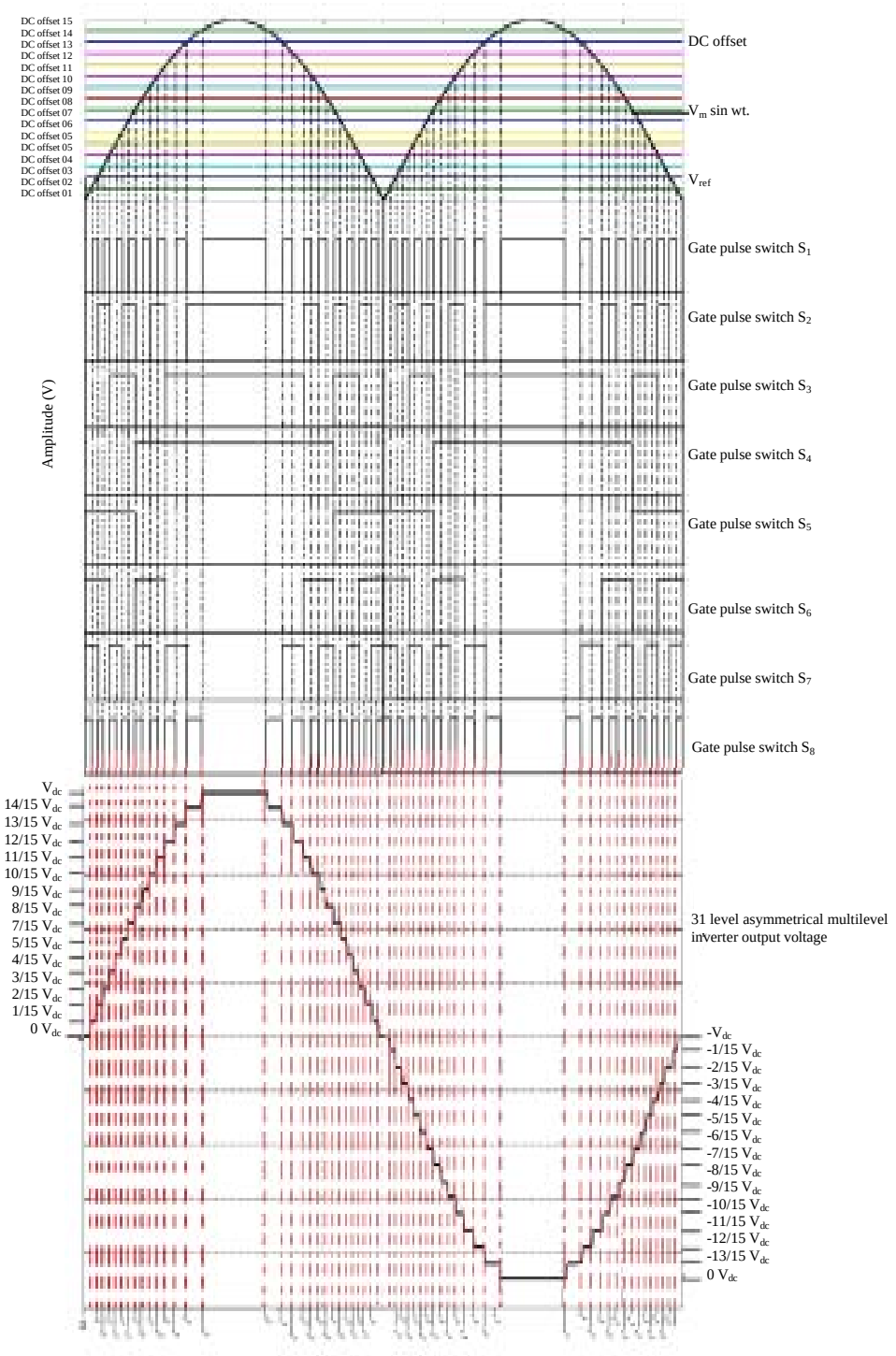

Fig. 4: Switching combination of 31-level inverter

$$A_j = \int_0^{\theta_j^1} mV_{dc}\sin(wt)d(wt) + \int_{\theta_{j1}^1}^{\pi/2} jV_{dcd}(wt) - \sum_{i=1}^{j-1} A_j \qquad (10)$$

Figure 4 shows the switching combination of asymmetrical cascaded H bridge multilevel inverter. In this circuit the low frequency pulse width modulation is used for controlling the switches in 31-level asymmetrical inverter. The DC offset is compared with the absolute sine wave. Depending upon the logical circuit like AND, OR, NOT, etc., the switching technique is used for generating the gate pulse. In the system, the output level is positive

15 level, negative 15 level and zero level one. According to this the 15 DC offset are generated and compared with absolute sine wave to produce the switching pulse from switch S_1-S_8.

In next step shows the output voltage level of 31 level asymmetrical inverter. The output voltage level are 15 V_{dc}, 14 V_{dc},13 V_{dc}, 12 V_{dc}, 11 V_{dc}, 10 V_{dc}, 09 V_{dc}, 08 V_{dc}, 07 V_{dc}, 06 V_{dc}, 05 V_{dc}, 04 V_{dc}, 03 V_{dc}, 02 V_{dc}, 01 V_{dc}, 00 V_{dc}, -01 V_{dc}, -02 V_{dc}, -03 V_{dc}, -04 V_{dc}, -05 V_{dc}, -06 V_{dc}, -07 V_{dc}, -08 V_{dc}, -09 V_{dc}, -10 V_{dc}, -11 V_{dc}, -12 V_{dc}, -13 V_{dc}, -14 V_{dc} and -15 V_{dc}.

RESULTS AND DISCUSSION

Figure 5-10 shows the switching gate pulse for 31-level asymmetrical cascaded multilevel inverter. This switching technique are design by using DC offset of low frequency pulse width modulation. To reduce the switching losses in the system the low frequency pulse width modulation has implemented in this switching technique.

The output voltage of 31-level inverter as shown in Fig. 11. The output voltage levels are 15 V_{dc}, 30 V_{dc}, 45 V_{dc}, 60 V_{dc}, 75 V_{dc}, 90 V_{dc}, 105 V_{dc}, 120 V_{dc}, 135 V_{dc}, 150 V_{dc}, 165 V_{dc}, 180 V_{dc}, 195 V_{dc}, 210 V_{dc}, 225 V_{dc},0 V_{dc}, -15 V_{dc}, -30 V_{dc}, -45 V_{dc},- 60 V_{dc}, -75 V_{dc}, -90 V_{dc}, -105 V_{dc}, -120 V_{dc}, -135 V_{dc}, -150 V_{dc}, -165 V_{dc}, -180 V_{dc}, -195 V_{dc}, -210 V_{dc}, -225 V_{dc}, respectively. The total harmonics distortion for 31-level inverter is 3.25% (Jayapalan and Edward, 2017).

Hardware: The real time implementation of 31-level inverter using PIC16F877A microcontroller with RL load as shown in Fig. 12. In this system, the PIC16F877A Microcontroller are used for generating gate pulse to control the MOSFET switch in the inverter. The MOSFET Driver circuit is used to step up the gate voltage

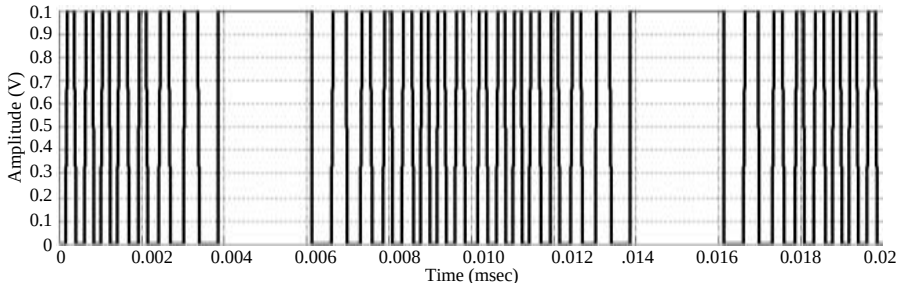

Fig. 5: Gate pulse for switch S_1

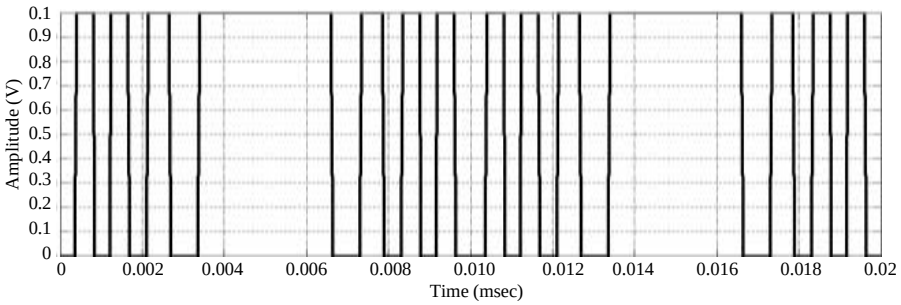

Fig. 6: Gate pulse for switch S_2

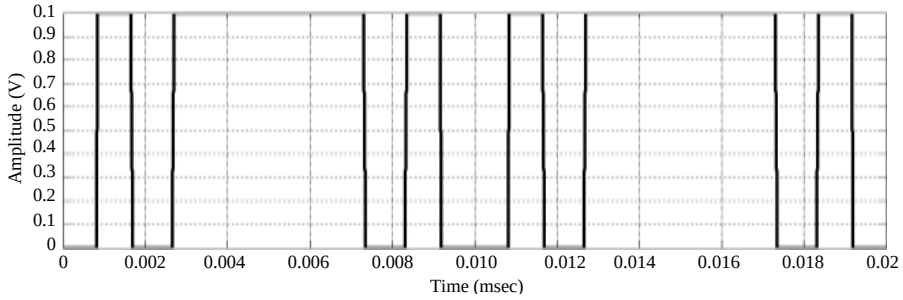

Fig. 7: Gate pulse for switch S_3

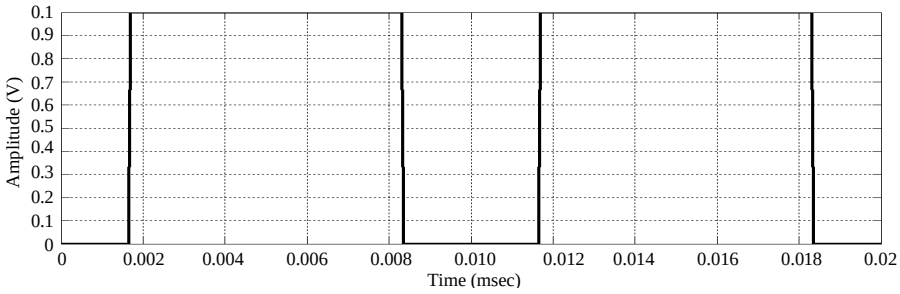

Fig. 8: Gate pulse for switch S_4

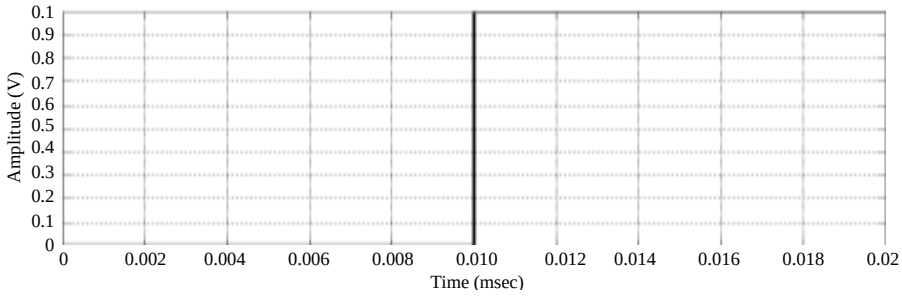

Fig. 9: Gate pulse for switch S_5 and S_6

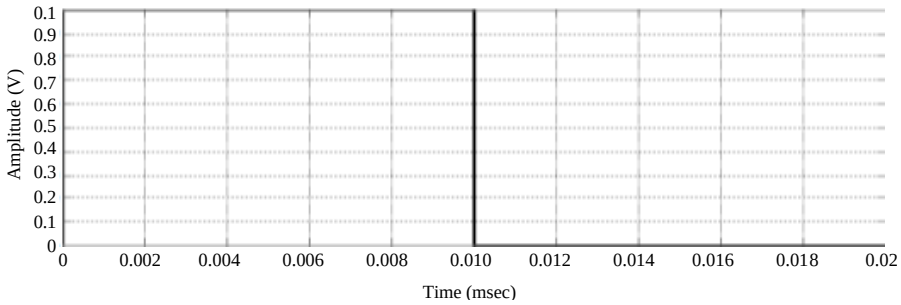

Fig. 10: Gate pulse for switch S_7 and S_8

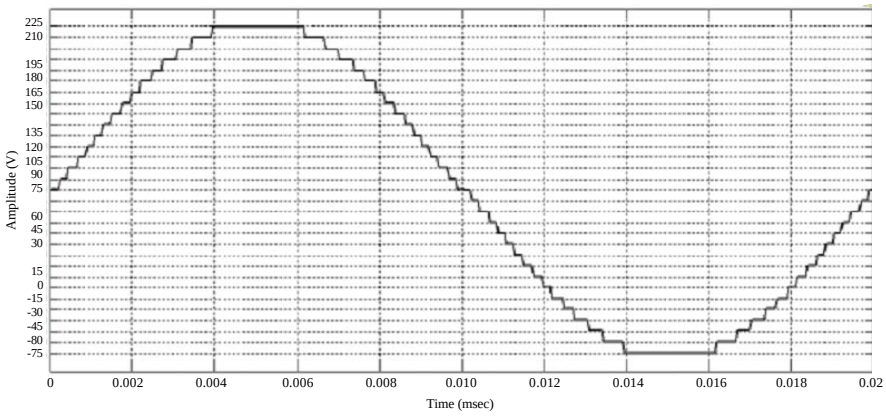

Fig. 11: Output voltage of 31-level asymmetrical MLI

form 5-12 V. The IRF640 Mosfet switch is used in the inverter circuit. The input DC voltage are 3 V_{dc}, 6 V_{dc}, 12 V_{dc} and 24 V_{dc} (Shankar and Edward, 2016a, b).

The output voltage and current waveform as shown in Fig. 13. The 31 level inverter using RL load which consists of resistance 100 Ω and inductance 5 mH. The output voltage for the inverter is 45 V_{dc}, 42 V_{dc}, 39 V_{dc},

36 V_{dc}, 33 V_{dc}, 30 V_{dc}, 27 V_{dc}, 24 V_{dc}, 21 V_{dc}, 18 V_{dc}, 15 V_{dc}, 12 V_{dc}, 9 V_{dc}, 6 V_{dc}, 3 V_{dc}, 0 V_{dc}, -3 V_{dc}, -6 V_{dc}, -9 V_{dc}, -12 V_{dc}, -15 V_{dc}, -18 V_{dc}, -21V_{dc}, -24 V_{dc}, -27 V_{dc}, -30 V_{dc}, -33 V_{dc}, -36 V_{dc}, -39 V_{dc}, -42 V_{dc}. The THD analysis for 31-level inverter as shown in Fig. 14. The THD is analyzed for 31 level inverter using RL load is 14.22%. In this system the first order

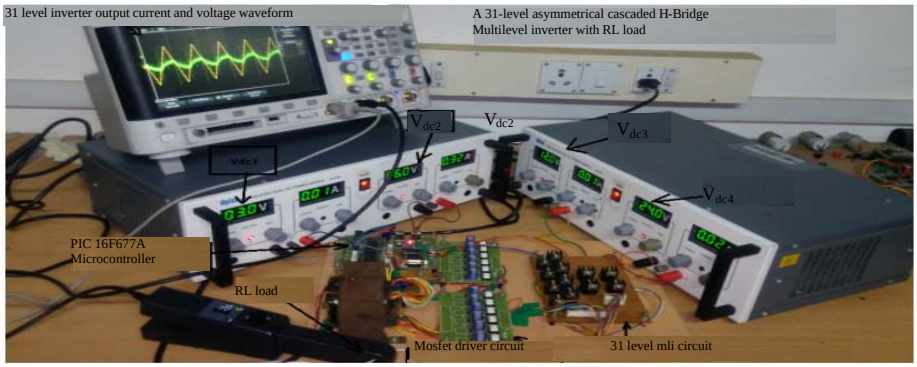

Fig. 12: Hardware implementation of 31-level inverter using RL load

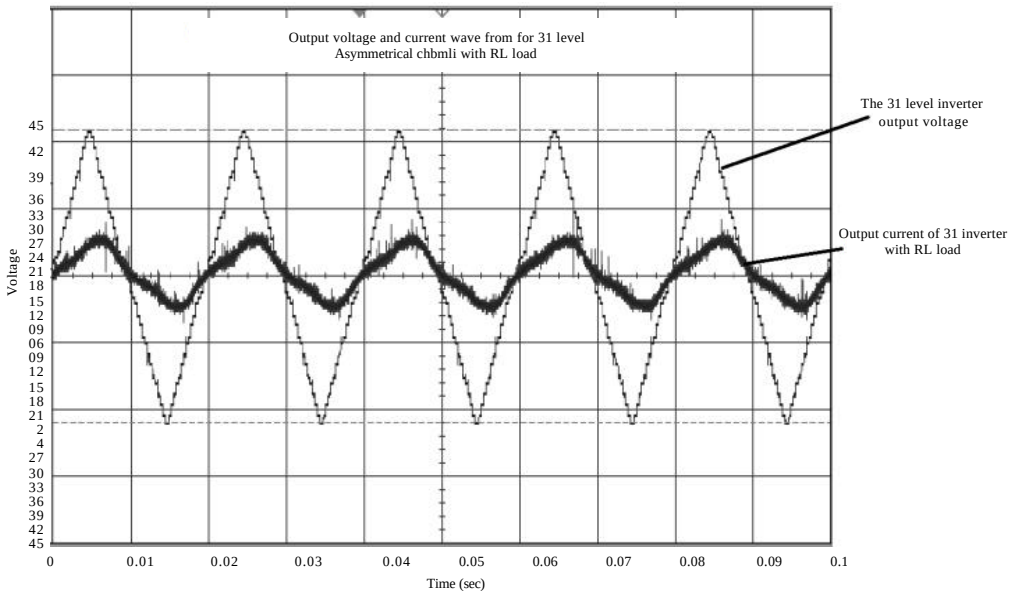

Fig. 13: Output voltage and current waveform for 31-level inverter using RL load

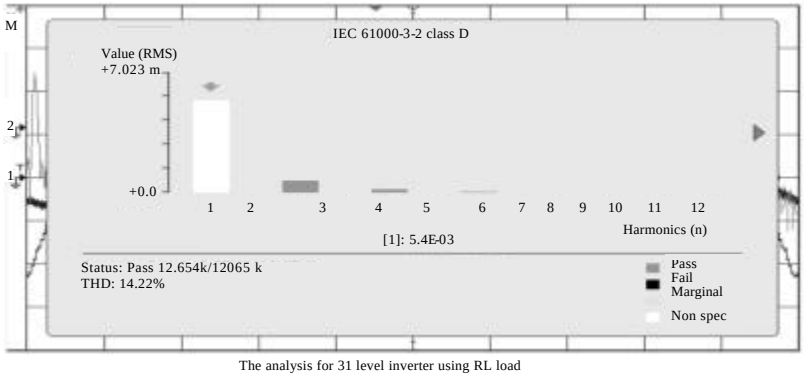

Fig. 14: THD analysis for 31-level inverter

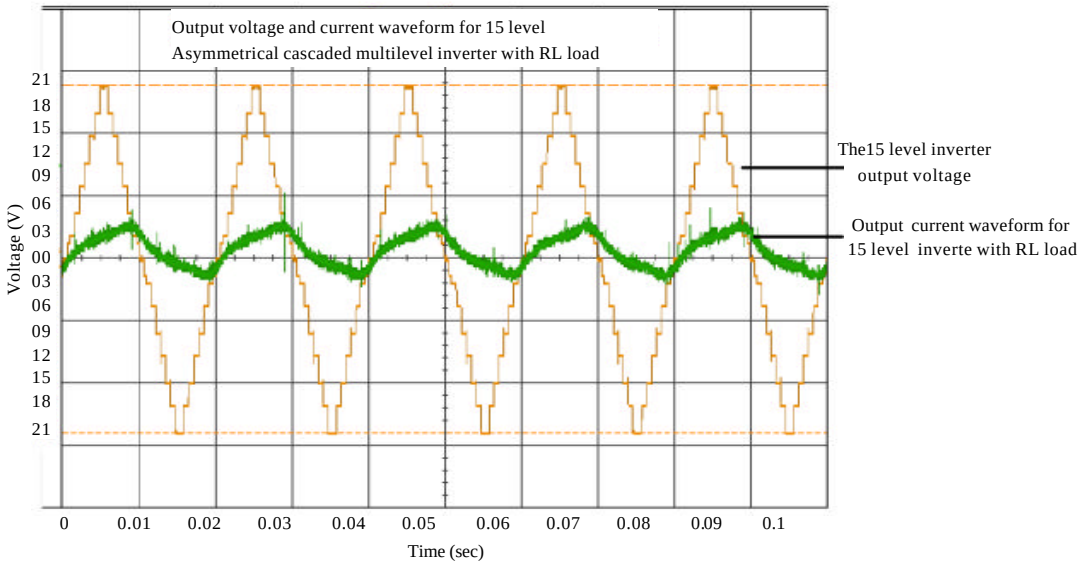

Fig. 15: Output voltage and current waveform for 15-level inverter using RL load

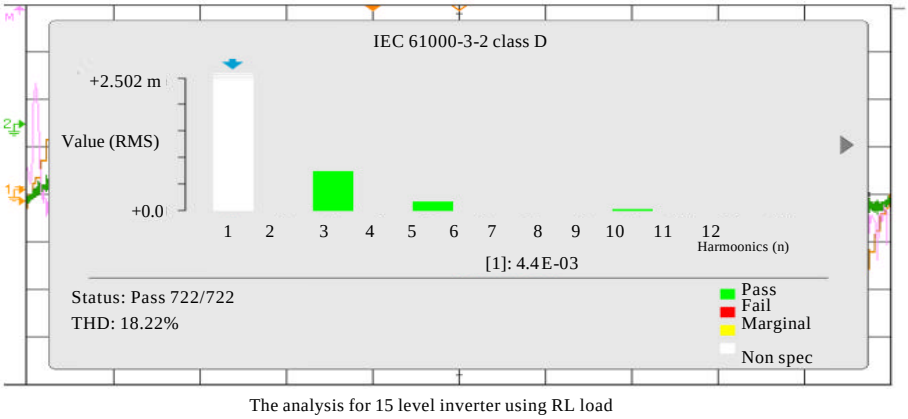

Fig. 16: THD analysis for 15-level inverter

harmonics is very high when compared with other harmonics. The output voltage and current waveform as shown in Fig. 15. The input DC voltage source for 15-level inverter is 3 V_{dc}, 6 V_{dc} and 12 V_{dc}. The 15 level inverter with RL load which consists of resistance 100 Ω and inductance 5 mH. The output voltage for the inverter is 21 V_{dc}, 18 V_{dc}, 15 V_{dc}, 12 V_{dc}, 9 V_{dc}, 6 V_{dc}, 3 V_{dc}, 0 V_{dc}, -3 V_{dc}, -6 V_{dc}, -9 V_{dc}, -12 V_{dc},-15 V_{dc}, -18 V_{dc} and -21 V_{dc}.

The THD analysis for 15 level inverter as shown in Fig. 16. The THD is analyzed for 31 level inverter using RL load is 18.22%. In this system, the first order harmonics and third order harmonics is very high when compared with other harmonics. While comparing the 15 and 31-level the third order harmonics is very high in 15 level.

CONCLUSION

The 15 and 31-level asymmetrical cascaded H bridge multilevel inverter are analyzed in this system. The low frequency pulse width modulation techniques is used for generating the gate pulse for inverter. In three DC voltage source are V_{dc1} = 3 V ,V_{dc2} = 6 V, V_{dc3} = 12 V used along with RL load to generate the 15 level inverter and THD is analyzed for 15 level inverter is 18.22% where as in the four DC voltage source are V_{dc1} = 3V, V_{dc2} = 6 V, V_{dc3} = 12 V and V_{dc} = 24 V used along with RL load to generate the 31 level inverter and the THD is analyzed for 31-level inverter is 14.22%. So the THD is reduce my increasing the levels. The THD for 31-level inverter is 14.22%. As per the THD analysis 31-level inverter is better performance of system.

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