Journal of Engineering and Applied Sciences 12 (20): 5116-5120, 2017

ISSN: 1816-949X

© Medwell Journals, 2017

Performance Analysis of Electrical Characteristics for Short Channel Effects (SCE) in Carbon Nano Tube Field Effect Transistor (CNTFET) Devices

G. Ramana Murthy, Ajay Kumar Singh, J. Hossen and P. Velrajkumar Faculty of Engineering and Technology, Multimedia University, Selangor, Malaysia

Abstract: This study presents the study of electrical characteristics performance of Carbon Nanotube Field Effect Transistor (CNTFET) devices in terms of modulated channel potential, surface potential, threshold voltage, threshold voltage roll-off and Drain Induced Barrier Voltage (DIBL) effect. From the study, it is evident that the modulated channel potential generally falls with drain voltage. The fall becomes steeper for higher intrinsic carrier concentration. Surface potential is suppressed with the channel for larger oxide thickness. Threshold voltage rises sharply when the channel length reduces below 6 nm whereas threshold voltage roll-off is severe for lower oxide thickness. DIBL effect is more predominant for nano-scale devices and becomes severe for larger oxide thickness due to poor coupling between the channel and the gate.

Key words: CNTFET, modulated channel potential, surface potential, threshold voltage roll-off, DIBL, evident

INTRODUCTION

Conventional silicon Metal Oxide Field-Effect Transistor (MOSFET) scaling has been phenomenal in recent years. The bottlenecks in scaling process needed other alternative measures to overcome Short Channel Effects (SCE) in MOSFETs. Carbon Nanotube Field Effect Transistor (CNTFET) is one of the most promising in today's research as a potential and alternative device to substitute the conventional MOSFETs due to its excellent I-V/C-V characteristics and exceptional control over SCEs. The research on CNTFETs is mostly at preliminary stage in terms of modelling of electrical parameter characteristics. Research models published on CNTFET were either mostly numerical based or self-consistency accomplishment type which cannot be implemented in SPICE Models directly (Paul et al., 2006; Marani and Perri, 2012). The compact analytical models for threshold voltage, surface potential and Drain Induced Barrier Lowering (DIBL) were earlier derived by Singh et al. (2015) and Kumar et al. (2015).

The continuous shrink in the size of device structures (<100 nm) increases the influence of the quantum mechanical effect (Lazaro et al., 2006; Wen and Singh, 2010). Besides tunnelling, the quantum confinement effect highly influences the performance of the CNTFET devices (Ahn and Shin, 2007; Sinha and Chaudhury, 2012). Extensive simulation tools based on the Non-Equilibrium Greens Function (NEGF) formalism have been developed in order to study the quantum

effects in CNTs (Datta, 2000; Wang et al., 2015). Although, NEGF is a powerful tool in modelling quantum effects in nano-structures but it is computationally very demanding. A variety of quantum mechanical effects such as quantization in density of states, tunnelling and quantum mechanical reflections can be captured by using coupled Poisson-Schrodinger (SP) (John et al., 2004; Pourfath et al., 2006) but this model encounters numerical difficulties. Since, classical simulation cannot cover quantum mechanical effect, researchers have proposed quantum correction models (Raychowdhury et al., 2004; Wagner et al., 2006; Raychowdhury and Roy, 2006).

In the present research, the behavior of modulated channel potential, surface potential, threshold voltage, threshold voltage roll-off and DIBL effects using proposed models has been studied. The modulated potential falls sharply with channel length and the fall is more visible for larger carrier concentration. The surface potential remains constant along the channel. The surface potential degraded due to larger oxide thickness. The rise in threshold voltage is evident when the channel length falls below 6 nm rises and threshold voltage roll-off becomes dominant for lower oxide thickness. In nanoscale CNTFET device, DIBL effect is more pronounced.

MATERIALS AND METHODS

Analytical models: The structure of the CNTFET is as shown in Fig. 1. There are three regions, namely; the source, drain and central regions. The central region,

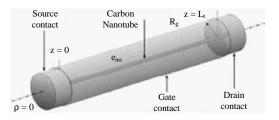


Fig. 1: Coaxial CNFET geometry (John et al., 2004)

known as channel, allows the movement of carriers from source to drain. Under quantum capacitance limit, poisson equation reduces to laplace equation as shown in Eq. 1:

$$\frac{\partial^2 \mathbf{v}}{\partial \rho^2} + \frac{1}{\rho} \frac{\partial \mathbf{v}}{\partial \rho} + \frac{\partial^2 \mathbf{v}}{\partial z^2} = 0 \tag{1}$$

By using the separation of variable technique and using appropriate boundary conditions, the potential in channel can be derived as shown in Eq. 2:

$$\begin{split} V(\rho,z) = & \frac{V_{gs} - \frac{\varphi_{G}}{q}}{J_{0}(\frac{r_{cnt}}{\lambda})} J_{0}(\rho\lambda) [(\frac{V_{bi} - V_{CNT}}{V_{GS} - \frac{\varphi_{G}}{q}} - \\ & (\frac{-V_{ds} - \left(V_{bi} - V_{cnt}\right)(1 - e^{\frac{L}{\lambda}})}{2(V_{GS} - \frac{\varphi_{G}}{q}) sinh(\frac{L}{\lambda})} e^{\frac{z}{\lambda}} + \frac{-V_{ds} - \left(V_{bi} - V_{cnt}\right)(1 - e^{\frac{L}{\lambda}})}{2(V_{GS} - \frac{\varphi_{G}}{q}) sinh(\frac{L}{\lambda})} e^{\frac{z}{\lambda}}] \end{split}$$
 (2)

Where:

 V_{bi} = The built-in-potential

 J_0 = The first kind of bessel function

V_{cot} = The modulated potential which is introduced to take account for the induced mobile charges in the channel due to applied gate voltage and modelled as shown in Eq. 3

$$V_{cnt} = V_{ss} - [\alpha_1(1-\tilde{\lambda}_1)]$$
(3)

Where:

 $\alpha = In \left[1 + \beta (V_{ds}/V_t)\right]$

 $\begin{array}{ll} \tilde{\chi}_1 &=& 1\text{-}[\alpha(1\text{-}e^{\nu_{\mathfrak{g}}/\nu_{\tau}})] \\ V_t &=& The \; thermal \; voltage \end{array}$

 β = The fitting parameter

Equation 2 describes the behaviour of the electric fields along the surface in CNTFET devices. In the ballistic region the surface potential can be obtained by substituting $\rho = r_{cnt}$ in Eq. 2.

The minimum potential in the ballistic region is obtained using $\partial \phi_s/\partial_z = 0$. Using the standard definition of threshold voltage used for the conventiona MOSFET, the threshold voltage for CNTFET devices can be derived as shown in Eq. 4:

$$V_{th} = \frac{a_{11}}{2} \left[-1 + \sqrt{1 + 4(\frac{a_{12}}{a_{11}^2})} \right] \tag{4}$$

Where:

$$\frac{a_{_{12}}}{a_{_{11}}^{^{2}}} = \frac{[2\Phi_{_{B}} + V_{_{ds}} + V_{_{bi}} (1 - \lambda_{_{13}} + e^{\frac{1}{\lambda_{\lambda}}})][\frac{V_{_{bi}}}{2\beta 1} - 1]}{[2 - \lambda_{_{13}} - e^{\frac{1}{\lambda_{\lambda}}} + \lambda_{_{14}}V_{_{bi}}]^{2}}$$

Threshold voltage-roll off is defined as the difference between the threshold voltage value of the long channel to that of short channel.

 Δv_{th} is threshold voltage of the long channel threshold voltage of the short channel. It is observed that at V_{ds} = 0, ΔV_{th} can be mostly controlled with the channel Length (L), gate source voltage (V_{gs}) and (V_{bi}).

In short channel effect, the phenomena of DIBL is unavoidable. In long channel effect, the drain current is controlled by gate voltage whereas as when the channel length is reduced, the drain voltage play an important roles to dominate the control of channel which is known as DIBL effect. The DIBL equation has been derived by using relation as shown in Eq. 5:

DIBL =
$$\frac{V_{th} (V_{ds} = 1 \text{ V}) - V_{th} (V_{ds} = 0.05 \text{ V})}{V_{ds} (1 \text{ V}) - V_{ds} (0.05 \text{ V})}$$
(5)

Using the expression as the suggested by Fregonese et al. (2009), the analytical expression for drain current l_{DSDT} in the ballistic transport region has been derived as shown in Eq. 6:

$$\begin{split} I_{\mathrm{DSDT}} &= \frac{4q}{h} KT [ln\{1 + e^{\frac{\cdot ((\Delta p_1 \cdot qV_{\mathrm{cut}}))}{KT}} - \\ &ln\{1 + e^{\frac{\cdot ((\cdot (\Delta p_1 \cdot qV_{\mathrm{cut}} + qV_{d_s})}{KT}}\} + ln^{\frac{(1 + e^{\frac{\cdot qV_{d_s}}{KT}})}{2}}] \end{split} \tag{6}$$

Where:

 The energy of first sub-band in CNT (KT/q) = The thermal voltage

The pre-factor 4 is included to consider the double degeneracy of the first sub-band and electron spin. The 3rd term on the RHS of Eq. 6 is the extra contribution due to assumption of unitary transmission coefficient. This term is dominating factor in the nano-scale CNTFET devices.

RESULTS AND DISCUSSION

The modulated potentialis used to take account for the induced mobile charges due to applied gate voltage. Figure 2 shows the computed numerical data of V_{cnt} for three different values of n_i (r_{cnt} = 3 nm) against V_{ds} . The modulated potential falls with V_{ds} irrespective of n_i . The fall is further supported by larger value of n_i due to increased channel concentration.

The variation of surface potential with channel length for different oxide thickness is shown in Fig. 3. The general behaviour of the potential is to fall for larger for $L \le 3$ nm. The surface potential shows slight variation for channel length L > 3 nm. The effect of oxide thickness on surface potential of nano-scale CNTFET devices is almost negligible whereas for larger channel length surface potential supressed at larger oxide thickness due to weak coupling between channel and gate.

In channel region, the surface potential remains constant along the channel irrespective of the carrier concentration. However, for larger carrier concentration it is noticed that surface potential takes smaller value as in Fig. 4 due to reduced modulated channel potential.

From the observation of the result of threshold voltage it is observed that when channel length decreases (L \leq 6 nm), the threshold voltage increases sharply. This increase of threshold voltage leads to a lower leakage power in the device. For lower applied V_{gs} value a lower threshold voltage is observed. For the channel length (L \geq 6 nm) it is noticed that the threshold voltage gives no changes with respect to the channel length as shown in Fig. 5.

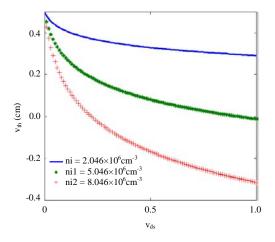


Fig. 2: V_{cnt} versus V_{ds}

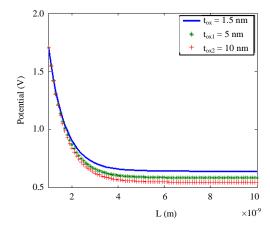


Fig. 3: Surface potential versus channel length

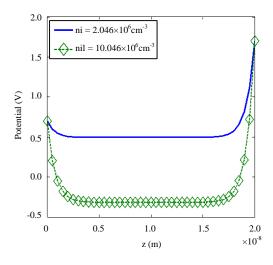


Fig. 4: Surface potential variation along channel

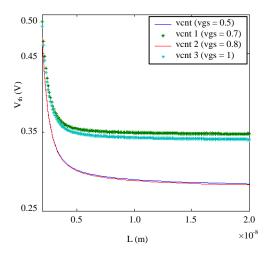


Fig. 5: Threshold voltage versus channel length

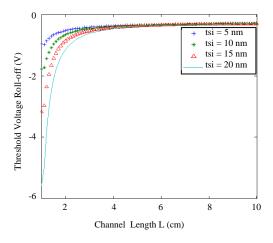


Fig. 6: Threshold voltage roll off versus channel length

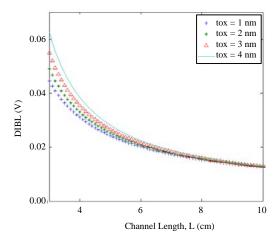


Fig. 7: DIBL versus channel length

At lower oxide thickness, lower value of threshold voltage roll-off is observed. For larger length of CNTFET devices no effect of oxide thickness is observed on the threshold voltage roll-off as shown in Fig. 6.

Using Eq. 5 DIBL is calculated for CNTFET device at different oxide thickness as in Fig. 7. The short channel effects are more pronounced in nano scale devices compared to the large devices. Due to weak coupling between channel and gate the DIBL is further aggravated for larger oxide thickness due to weak control of gate over channel.

CONCLUSION

This study presents the behavior of modulated channel potential, surface potential, threshold voltage, threshold voltage roll-off and DIBL effect in CNTFET devices using proposed analytical models. The modulated potential falls with drain-source voltage due to increase channel concentration. Surface potential also tends to become small with respect to channel length due to reduced modulated potential. Threshold voltage increases sharply when the channel length is below 6 nm but shows no noticeable variation when the channel length is increased. Oxide thickness shows no impact on threshold voltage roll-off. DIBL becomes more predominant when the oxide thickness increases.

REFERENCES

Ahn, C. and M. Shin, 2007. Quantum simulation of coaxially gated CNTFETs by using an effective mass approach. J. Korean Phys. Soc., 50: 1887-1893.

Datta, S., 2000. Nanoscale device modeling: The Green's function method. Superlattices Microstruct., 28: 253-278.

Fregonese, S., C. Maneux and T. Zimmer, 2009. Implementation of tunneling phenomena in a CNTFET compact model. IEEE. Trans. Electron. Devices, 56: 2224-2231.

John, D.L., L.C. Castro, P.J.S. Pereira and D.L. Pulfrey, 2004. A schraodinger-poisson solver for modelling carbon nanotube FETs. NSTI. Nanotech, 3: 65-68.

Kumar, B.N., A.K. Singh, C.M.R. Prabhu, C. Venkataseshaiah and G.C. Sheng, 2015. Compact analytical model for one dimensional Carbon Nanotube Field Effect Transistor (CNTFET). ECS. Solid State Lett., 4: M12-M14.

Lazaro, A., B. Nae, O. Moldovan and B. Iniguez, 2006. A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations. J. Appl. Phys., 100: 1-12.

Marani, R. and A. Perri, 2012. Simulation of CNTFET digital circuits: A Verilog-A implementation. Int. J. Res. Rev. Applied Sci., 11: 74-81.

Paul, B.C., S. Fujita, M. Okajima and T. Lee, 2006. Modeling and analysis of circuit performance of ballistic CNFET. Proceedings of the ACM DAC, July 24-28, 2006, ACM New York, USA., pp. 717-722.

Pourfath, M., H. Kosina and S. Selberherr, 2006. A fast and stable poisson-schrodinger solver for the analysis of carbon nanotube transistors. J. Comput. Electron., 5: 155-159.

Raychowdhury, A. and K. Roy, 2006. Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies. IEEE. Trans. Comput. Aided Des. Integr. Circuits Syst., 25: 58-65.

Raychowdhury, A., S. Mukhopadhyay and K. Roy, 2004.

A circuit-compatible model of ballistic carbon nanotube field-effect transistors. IEEE. Trans. Comput. Aided Des. Integr. Circuits Syst., 23: 1411-1420.

- Singh, A.K., B.N. Kumar and C.M.R. Prabhu, 2015. Study of Drain Induced Barrier Lowering (DIBL), threshold voltage roll-off and drain current in Carbon Nanotube Field-Effect Transistor (CNTFET). ECS. J. Solid State Sci. Technol., 4: M69-M72.
- Sinha, S.K. and S. Chaudhury, 2012. Oxide thickness effect on quantum capacitance in single-gate MOSFET and CNTFET devices. Proceedings of the Annual IEEE Conference on India (INDICON), December 7-9, 2012, IEEE, New York, USA., ISBN:978-1-4673-2270-6, pp. 42-46.
- Wagner, M., M. Karner, J. Cervenka, M. Vasicek and H. Kosina *et al.*, 2006. Quantum correction for DG MOSFETs. J. Comput. Electron., 5: 397-400.
- Wang, W., H. Wang, J. Liu, N. Li and T. Zhang et al., 2015. Performance analysis of an ultralow power circuit using single halo CNTFETs. Semicond. Sci. Technol., Vol. 30,
- Wen, T.P. and A.K. Singh, 2010. A comprehensive analytical study of an undoped symmetrical double-gate MOSFET after considering quantum confinement parameter. Microelectronics J., 41: 162-170.