Journal of Engineering and Applied Sciences 12 (14): 3793-3797, 2017
ISSN: 1816-949X

Novel Nine-Transistor (9T) SRAM for Read/Write Operation

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Abstract: On-chip cache utilizes an enormous percentage of the entire chip region and spread with very fast rate in advanced technologies. Cell stability and low power SRAM are the major concerns and has become a crucial component in modern VLSI systems. Low power SRAM array is fundamental to organize substantial reliability and prolonged battery life for portable application. Since, charging/discharging enormous bit lines capacitance consume large portion of power, new SRAM design is proposed to lessen the power consumption and access delay for read/write operation. Single bit line technique performed in the proposed circuit lead to power consumption reduction during write operation about 79% and separate path used for read operation reduces the power consumption about 49.1% compared to 6T cell. Separate path during read operation and connecting/disconnecting the feedback path during write operation decrease the delay time and hence lessen the power consumption throughout read/write operation. The read/write stability is maintained in the proposed Novel 9T SRAM cell. The designed cell can be utilized in mobile appliances even in worse temperature state with lower power consumption.

Key words: SRAM, power consumption, access time, read/write, stability, SNM

INTRODUCTION

In every aspect of our daily lifestyle the portable gadgets such as personal digital assistants and mobile appliances are obtaining more popularity while making improvements day by day (Liu *et al*., 2007). Higher demand in fixed memory access in image or video implementations affects its power consumption making lifetime of the battery reach its limitation. Power dissipation has become a vital consideration due to the rapid development of battery operated tools and appliances (Powers, 1995; Gopal *et al*., 2013). Current leakage is increasing with the shrinking of the device size. Therefore, low power SRAM cell design is crucial in order to accomplish battery operated device functions (Alioto, 2012). SRAMs made up of almost 90% of VLSI circuits. Important factors of SRAMs which are the speed, stability and power consumption have led to various designs with the objective of reducing the power utilization to the minimum level during read/write operations (Grossar *et al*., 2006). Stability is another key factor in SRAM cell design. It decides the cell's ability to operate the tolerances and processing constrain. Correct operations have to be maintained in the presence of noise signals. Thus, various studies and experimentation have been done in order to minimize the power consumption of SRAM modules. One of the most functional steps to meet this purpose is to create an extreme low power SRAM design. Latest research works have proved that access disturbance at low-power mode in Conventional 6T SRAM caused it to suffers extreme stability degradation (Seevinck *et al*., 1987).

The aim of this study is to design an improved Novel 9T SRAM cell in 65 nm CMOS technology which can perform the read/write operation in low power state by improving the static noise margin (Aly and Bayoumi, 2007). The proposed design works by detaching the feedback path of the respective inverter so that the desired writing state can be achieved. The write operation is executed effortlessly by transferring the data from the bit-line to storage node and this will cause reduction in power consumption and access time.

This study evaluates the following features for SRAM cell using the proposed novel 9T SRAM design: power consumption, write/read access time area/stability and static noise margin. The results, output and simulations are compared with conventional 6T SRAM cell to differentiate the high performance of the proposed cell.

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MATERIALS AND METHODS

Proposed novel 9T SRAM design: Schematic design of the proposed Novel 9T SRAM cell is shown in Fig. 1. The cell contains nine transistors including two bridging transistors (NMOS-N5 and PMOS-P3) which are connected at the feedback path of the inverter and a read access transistor which only been activated during read operation (NMOS-N6). The write execution of the suggested cell differs from 6T SRAM by cutting off the feedback path of the two inverters. Thus, excess transistor's working load is eliminated by reducing its power consumption and access delay. Besides that the two bridging transistors are operated by one of the Bit-Line (BL) to further decrease the power consumption of the cell. Therefore, the access time is shortening since the switching operation at the feedback path is executed simultaneously when N5 is turned ON while P3 is turned OFF and vice versa. These bridging transistors act as feedback path transistor in order to execute immediate state change (0->1 or 1->0) at storage nodes Q and nQ without discharging completely. Two word line signals (WL and nWL) controls the write access transistor to enable write '0' or write '1' operation. A read access transistor (N6) activated by read line signal (RWL) is used for read operation which shortens the read path.

The write operation is done by shifting the data from bit-lines (BL and nBL) to storage nodes (Q and nQ). The cross-coupled inverter's path is cut-off by the bridging transistor before executing any write operation. Before begin writing both the bit-lines is set to the desired logic and by enabling the access transistors. nBL carries complement of the input data of BL so that when BL is equal to 1 then nBL is equal to 0 and vice versa. During each operation the bridging transistor will ON/OFF alternatively by the input from BL. The activated transistors during both write operation is shown in Fig. 2 and 3.

For write '0' operation at storage node Q, bit-line nBL has to be set at 1 (nBL=1). BL carries complement of the input data (BL = 0). Since, BL is set to 0, transistor N5 is kept OFF while transistor P3 is kept ON initially. The transistor N4 is turned OFF by setting nWL to "0" which disconnects BL from inverter 1 (P1 and N1). Next, the transistor N3 is turned ON by using WL to "1". Once N3 is ON, the data form nBL is transferred to storage node Q2 through inverter 2 (P2 and N2) to change Q which equals Q1.

For write '1' operation at storage node Q, bit-line BL has to be set at 1 (BL = 1). nBL carries complement of the input data (nBL = 0). Since, BL is set to 1, transistor N5 is kept ON while transistor P3 is kept OFF initially. The transistor N3 is turned OFF by setting WL to "0" state

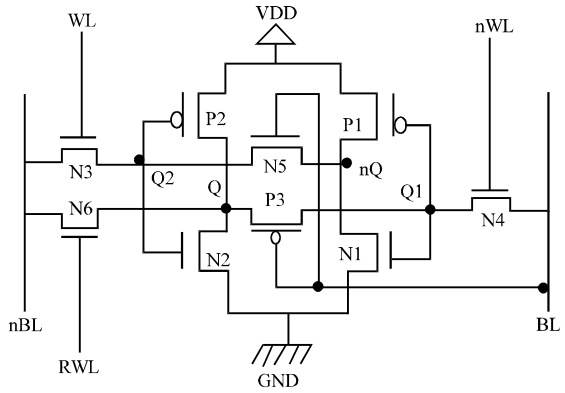

Fig. 1: Overall proposed circuit design

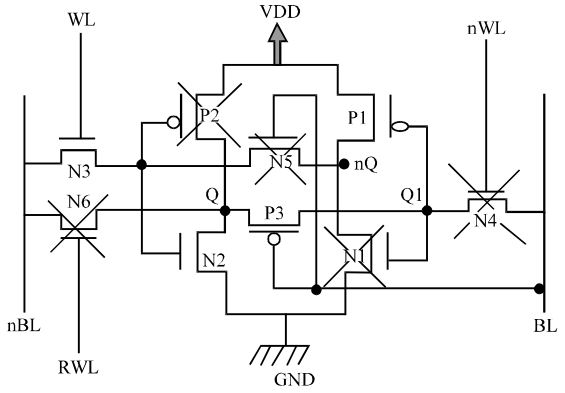

Fig. 2: Overall proposed circuit design 'O' operation

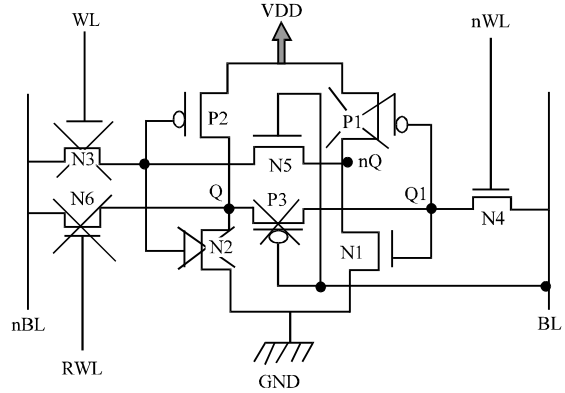

Fig. 3: Overall proposed circuit design '1' operation

which disconnects nBL from inverter 2 (P2 and N2). Then, the transistor N4 is turned ON by using nWL to "1". Once N4 is ON, the data from BL is transferred to storage node Q through inverter 1 (P1 and N1) to change nQ which equals Q2. A read operation (RWL = high, WL/nWL = 0); two transistors (N6 and N2) are used to perform the read mode.

RESULTS AND DISCUSSION

The Novel 9T cell architecture is implemented and simulated using 65 nm CMOS technology using BSIM4 model parameter. The supply voltage V_{DD} is 0.7 V. The proposed cell has two separate circuit for read and write operation in order to improve the speed, power consumption, stability and access time. Besides that the write circuit consists of two additional transistors which responsible for cutting off the feedback path of the inverters. Thus, the storage node states can be flipped during the write operation without discharging the bit-lines completely.

Table 1 show the simulated results of write power consumption for different inputs. From the output we can say that the overall power consumption of the designed novel 9T cell is much lower contrast with conventional 6T and 7T SRAM cell. Cutting off the feedback loop during write '1' and write '0' operation results in reduction in power consumption. Power consumption during transition 0->1 is decreased up to 81.96% and transition 1->0 is 81.84% compared to 6T SRAM. In transition 1->1 and 0->0 the power consumption is almost to 76%. Table 2 shows the write access time (write delay) which is defined as the time between the activation 50% of WL to Q bar is 90% of its swing. From Table 2, we can clearly observe that the access time of the designed novel 9T cell is reduced almost half contrast with 6T SRAM cell where the percentage value for transition 0->1 and 1->0 are 53.13 and 51.56%, respectively. The simulated result is illustrated in Fig. 4 where the output value for both the transition is reduced to half contrast with 6T SRAM.

The proposed 9T circuit is simulated at different temperature ranging from -20 to -140°C to observe its standby power. The sub-threshold current is controlled by carrier diffusion, thus leakage power increases exponentially with temperature. Compared to 6T SRAM, the standby powers at each temperature of the novel 9T cell design is <50% as illustrated in the bar graph above. Unlike in 6T SRAM cell, the standby power (hold power) of the designed cell is much lower which enables the cell to be operated under rough condition with low power consumption which is proven from the simulation result in Fig. 5.

Introducing a separate transistor (N6) at nBL and signal RWL enable the proposed circuit to execute read operation in different path than the write operation. At node Q, during read '0' nBL discharged through N2 and during read '1' nBL does not discharge since it is in same voltage level at node Q. Figure 6 explains that only one path of the execution consume power which is for read '1'

Table 1: Write for different input

Transitions	6T	7T	9T
Write power consumption (µw)			
0→1	4.938	5.073	0.891
1→1	0.017	0.018	0.004
1→0	4.944	0.987	0.898
0→0	0.016	0.004	0.004

Table 2: Write access time

Transitions	6T	7T	9T
Access time (Psec)			
0→1	128	136	60
1→0	128	62	62

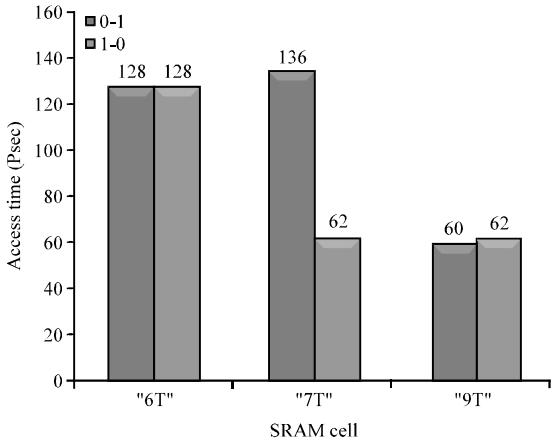

Fig. 4: Grahical representation of write access time

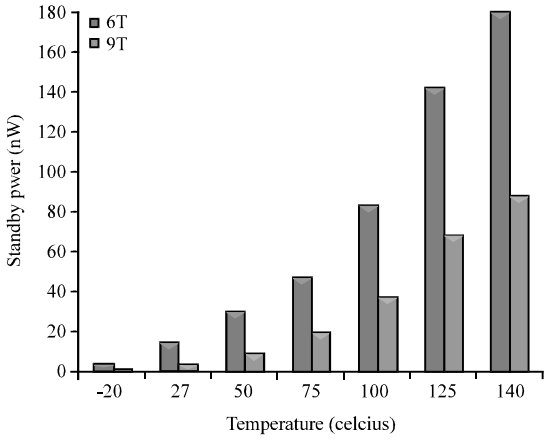

Fig. 5: Graphical representation of standby power at different temperature

whereas for read '0' the power consumption is nearly 0. Due to the reason, the access time for read '0' operation is also dropped drastically compared to 6T and 7T cell as shown in Fig. 7. Because of lower voltage drop on the read bit-line, the average percentage of read power reduction is 49.1% compared to the other cells. From the bar graph in Fig. 8 shown the read power consumption at temperature ranging from 27-140°C is about half (50%)

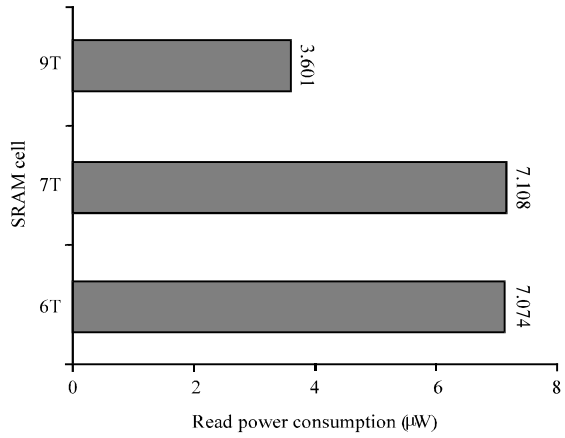

Fig. 6: Graphical representation of read power

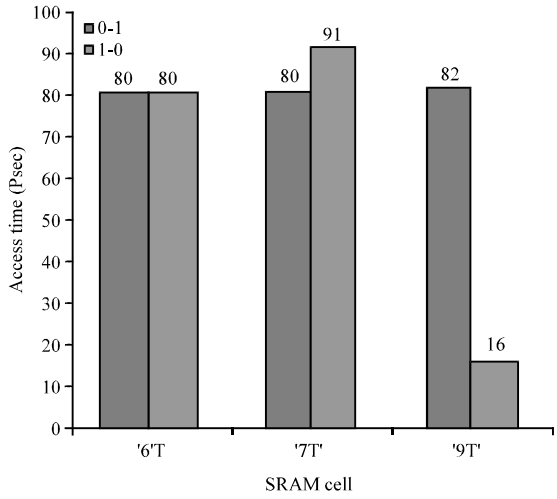

Fig. 7: Graphical representation of read access time for read '1' and '0'

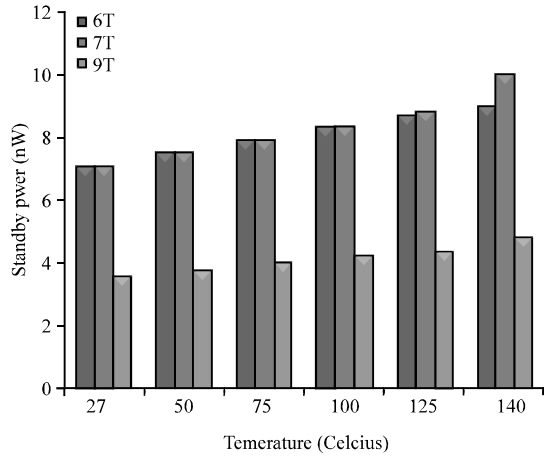

Fig. 8: Graphial representation of read power at different temperature

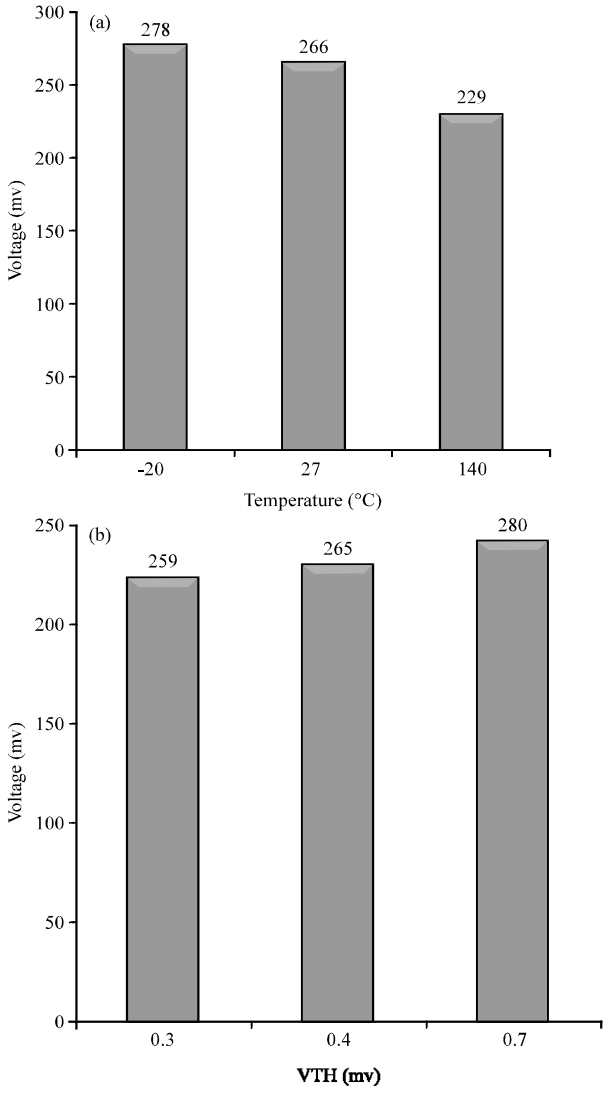

Fig. 9: a) Graphical representation of SNM for diffrernt temperature and b) graphical representation of SNW for different V_{TH}

of the other two cells. Due to individual read and write circuit path, the SNM of the Novel 9T cell is higher contrast with 6T SRAM as illustrated in Fig. 9a. The decrease in SNM value for the tested temperature range (-20 to 140°C) is only 17.6% because of carrier diffusion which increase the change in current when temperature increases. Figure 9b shows the read SNM at different threshold voltage (V_{TH}). At V_{TH} = 0.4, the SNM value of proposed design is 265 mV compared to 75 mV in 6T SRAM. The changes in SNM from low to high V_{TH} is about 7.5%. Slight variation occurs due to leakage current in the circuit. Overall, this shows that the cell

obtains higher stability because of the proposed design which consists of independent operation for read and write.

CONCLUSION

The proposed novel 9T SRAM reduces power consumption for both read and write operation by 49.1% and 79%, respectively. Based on the simulation output results, the proposed circuit allows reduction in access time delay and able to operate at worse condition (T = 140°C). The objective of the paper is achieved by presenting a new technique where the original circuit is introduced with two bridging transistors which are controlled by one of the bit-line itself. Connecting and disconnecting the feedback path alternatively without providing separate signal to the bridging transistors have sustain power during write operation as well minimizes the access delay. Separate path for read operation enhance the read stability, access delay and power consumption. Therefore the proposed 9T SRAM cell can be power efficient and provides high speed during read and write operation compared with conventional 6T SRAM.

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