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VLSI Implementation of Full Adder-Subtractor Design

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Abstract: Low power consumption and high performance in Very Large Scale Integration (VLSI) design are the major concerns in order to develop an efficient electronic devices. Addition is commonly used arithmetic operation in most electronic system which requires high performance and low power consumption of full adder circuit. This study aimed to design a low power and high performance full adder-subtractor by using Complementary Metal Oxide Semiconductor (CMOS) technology. Four design approaches of 4 bit Full Adder-Subtractor (FAS) static CMOS FAS with Pass Transistor Logic (PTL) XOR, static CMOS FAS with Transmission Gate (TG) XOR, PTL FAS and TG FAS circuit have been implemented in 90 nm CMOS technology using synopsys galaxy custom designer and compared in term of power consumption, power-delay product and area. PTL FAS able to reduce 27.7% of overall transistor count compared to both conventional static CMOS approach. For the 4 bit FAS design, PTL logic approach able to reduce 37.78% of area occupied and 27.78% of transistor count compared to static CMOS approaches. TG FAS has the lowest power consumption with 112.81 μW followed by PTL FAS with 133.34 μW, less than both conventional static CMOS approach. Results show that the PTL and TG approaches offer a low area and power consumption with a high performance of full adder-subtractor design.

Key words: Full adder-subtractor, CMOS, pass transistor, low power, low area

INTRODUCTION

Arithmetic operations are widely used in most electronic systems. Addition is a fundamental arithmetic operation and is the basic of many other commonly used arithmetic operations. The full adder cell is the most important and basis block of an arithmetic unit of a system. The design of 1 bit full adder which formed the basic building blocks of VLSI circuits intended to achieve a low transistor count and area occupied, minimized power consumption and increased the speed of the circuit by minimizing the delay (Ahmad and Hasan, 2011, 2013a, b, 2012; Chandra *et al*., 2015) as improving its performance directly leads to improve the performance of the whole system.

An adderis a digital logic circuit that performs addition of numbers. Adders are widely used in the arithmetic logic units and other part of the processor in many computer and many kinds of processors to calculate addresses, Table indices, adds binary numbers and accounts for values carried in as well as out. A 1 bit full adder adds three 1 bit numbers, often written as A, B and C_{in}. A and B are the operands and C_{in} is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders which add 2^n binary numbers where n = 1, 2, 3... The circuit produces a 2 bit output, output carry and sum typically represented by the signals C_{out} and sum.

Subtractor is a circuit which can be designed using the same approach as the adder. Implementation of subtractor from adder is usually to perform subtraction which involved two's complement notation. The 1 bit full subtractor is a combinational circuit which is used to perform subtraction of three 1 bit number. It has three inputs A (minuend) B (subtrahend) C (subtrahend) and two outputs D (difference) and B (borrow) (Ahmad and Hasan, 2013a). By, providing a control bit into a full subtractor circuit, it could performs addition for two's complement binary number (Ahmad and Hasan, 2013b). Thus, the full subtractor circuit can be modified into full adder-subtractor based on the control signal.

Down scaling the CMOS transistor has been the fundamental strategy for improving the performance of VLSI circuits for decades. However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits dictated by its operating principle (Ahmad and Hasan, 2012). The speed and power dissipation are the most important parameters which should be taken into consideration in digital circuits. Since, the number of integrated transistors become double

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once in 18 months, there is required to fabricate low power VLSI chips (Chandra *et al*., 2015). In this research, adder and subtractor are implemented into a single adder-subtractor circuit which could perform additionand subtraction operation with a control bit to switch the operation. After the implementation of the adder-subtractor circuit, few techniques were used to minimize the power consumption and increase the speed of the circuit in order to improve the performance of the circuit by minimizing the number of transistors and to implement some logic gate approaches such as pass transistor logic and transmission gate logic.

MATERIALS AND METHODS

Synopsys galaxy custom designer EDA Software is used for circuit simulation and layout design of each circuit. This user friendly software provides a wide range of powerful design guidance and automation from transistor level design to layout extraction and simulation. The 90 nm library CMOS technology file is used in designing the 4 bit full adder-subtractor. All simulations were carried out with 1.2 V supply voltage supply with 5 pF of load capacitance.

XOR gate: XOR gate plays an important role in designing the full adder-subtractor where the control signal is driven into an XOR gate before being fetched into the full adder. It acts as a selector between addition or subtraction by determining the control bit that drives into the gate. Many designs of 2-input XOR gates have been reported in order to enhance the performances (Ahmad and Hasan, 2011, 2013a, b; Chandra *et al*., 2015; Babu *et al*., 2014; Baghel and Rahi, 2015; Verma *et al*., 2014; Chowdury *et al*., 2015; Bazzazi *et al*., 2012). Two design approaches are used to implement XOR gate for this design which are Transmission Gate approach as in Fig. 1 and pass transistor logic approach as in Fig. 2 with minimum transistor count.

1 bit full adder: 1 bit full adder is another important component in the implementation of the full adder subtractor. Without the proper setup of the full adder circuit, the full adder-subtractor is unable to be achieved. Several design approaches which included static CMOS approach, transmission gate approach and pass transistor logic approach are used in the full adder implementation.

In implementing full adder-subtractor, three design approaches which includes of conventional fully static CMOS, Transmission Gate (TG) Logic and Pass Transistor Logic (PTL) are used to compare the functionality and

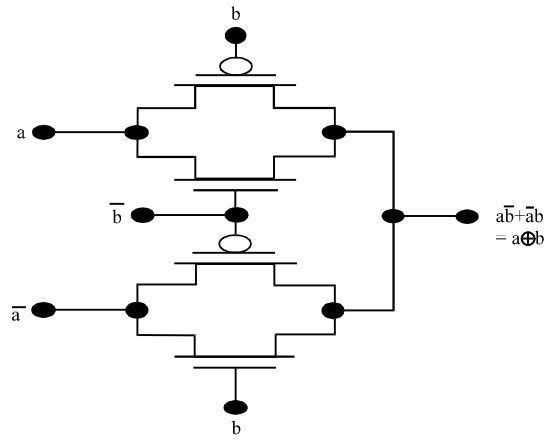

Fig. 1: Transmission gate XOR

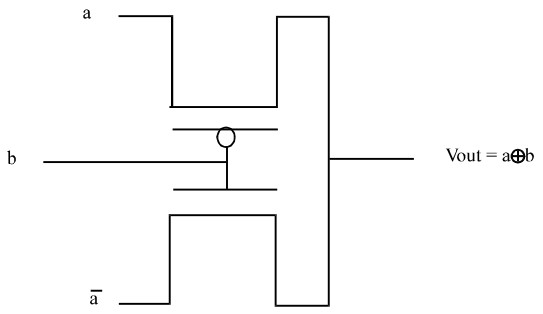

Fig. 2: PTL XOR

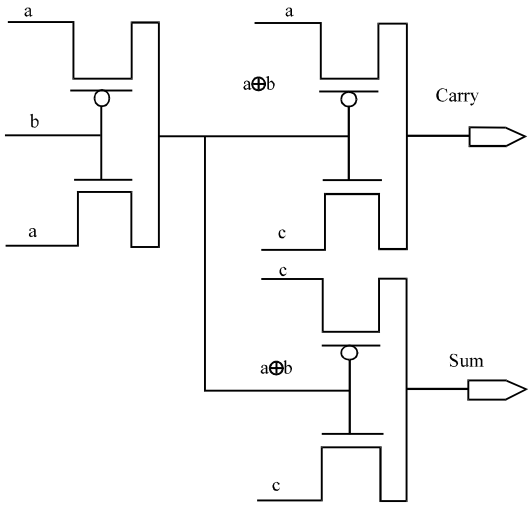

Fig. 3: PTL full adder

efficiency of each circuit. For PTL approach, the full adder-subtractor design is implemented by the 6 Transistors (6T) PTL full adder in Fig. 3. For TG approach, the full adder-subtractor design is implemented

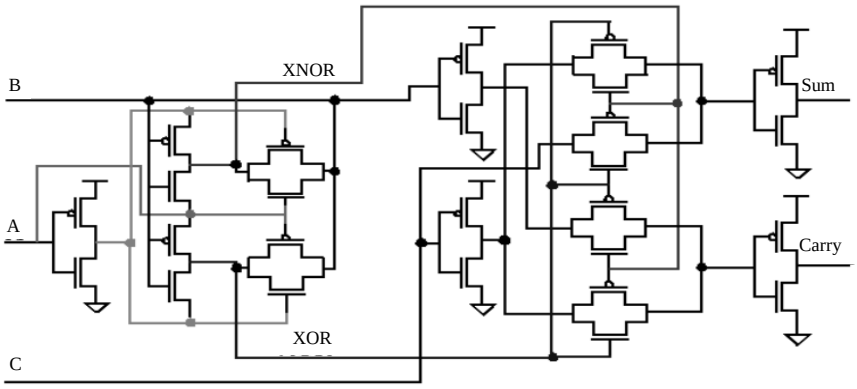

Fig. 4: TG full adder

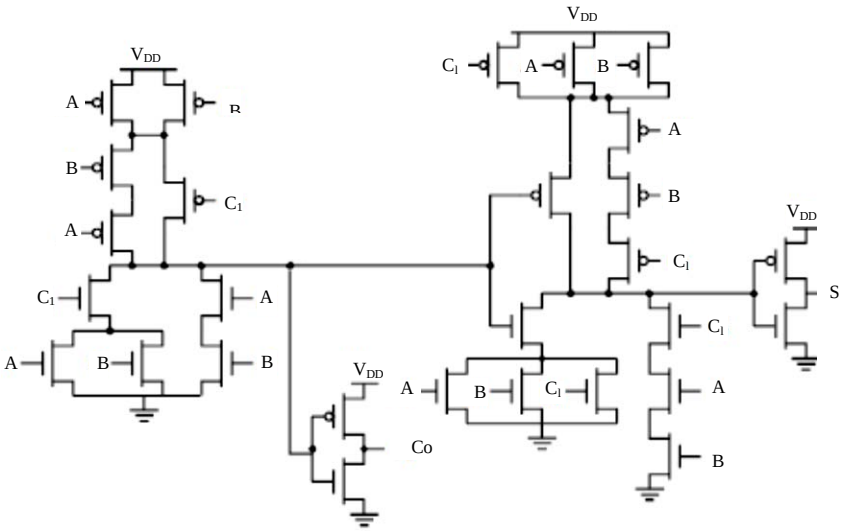

Fig. 5: Static CMOS full adder

by the 28 Transistors (28T) PTL full adder in Fig. 4. Generally, the 6T PTL full adder and TG full adder used are formed by three main MUXes circuit blocks. For static CMOS approach, the full adder subtractor design is implemented by the 28T static CMOS full adder in Fig. 5 which composed of complementary pull-down and pull-up networks in the circuit. These full adder circuits are modified into full adder-subtractor which able to perform addition and subtraction in a single circuit depends on the control signal by preceding a control signal into a XOR gate before driven into the full adder circuit.

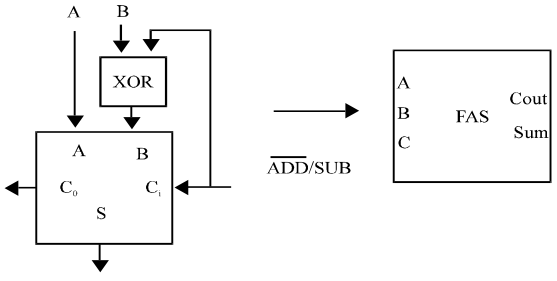

Fig. 6: 1 bit full adder-Subtractor design with XOR gate pre-fetch control signal

1 bit full adder-subtractor: Before the implementation of full adder-subtractor using PTL approach, conventional 28T static CMOS 1bit full adder is used to modify into full adder-subtractor by driving the input control signal, C_{in} and the input signal, B into an XOR gate and fetch the signal into the input B of the full adder block as shown in the block diagram in Fig. 6. The static CMOS full adder-subtractor design is used as a reference sample in comparing the power consumption and power-delay product with proposed PTL approach and TG approach.

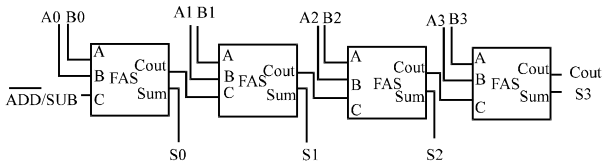

Fig. 7: 4 bit full adder-subtractor bolck diagram

As the carry-in signal in full adder-subtractor is high (logic "1"), the full adder-subtractor performs subtraction. While the carry-in signal is low (logic "0"), the full adder-subtractor performs addition. This is because the XOR gate has inverted the B signal whenever the carry-in signal is high. In this project, two design approaches are used to implement the XOR gate which are PTL and TG approaches. XOR gate acts as a signal control gate that able to fetch the signal of C_{in} and B.

4 bit full adder-subtractor: 1 bit Full Adder-Subtractor (FAS) is cascaded into 4 bit full adder subtractor by using four 1 bit full adder-subtractor blocks similar to the conventional method to cascade 4 bit carry look ahead full adder as shown in Fig. 7. Carry out for first three FAS block is driven into the carry-in of the FAS block next to it and bring forward the carry. The 4 bit binary input of A [A3, A2, A1, A0] and B [B3, B2, B1, B0] and a carry in signal are supplied into the 4 bit FAS. The result of the 4 bit FAS is in 5 bit binary form [Cout S3, S2, S1, S0] that is able to perform addition or subtraction depends on the carry in bit that acts as the control signal for overall circuit.

RESULTS AND DISCUSSION

The 4 bit full adder-subtractor are formed by cascading 4 circuit blocks of 1 bit full adder-subtractor. Four different design approaches are used to implement 4 bit full adder-subtractor in this study.

First, design approach is to cascade four 1 bit static CMOS full adder-subtractor with a pass transistor XOR gate as the signal control circuit inside each full adder-subtractor block. The output waveform is free from degradation problem. However, there are voltage spikes that can be clearly seen in the output waveform of the circuit that caused by the high current leakage due to the propagation delay during the transition state of the input signals. This circuit consumed 137.45 μm power and 443.96×10^{-16} J of power-delay product.

Figure 8 shows the layout of the 4 bit full adder-subtractor with PTL XOR. The area of the layout is 40.625×18.975 μm (770.859 μm^2). Second, design approach is to cascade four 1 bit static CMOS full adder-subtractor with transmission gate XOR gate as the signal control circuit inside each full adder-subtractor block to form a 4 bit static CMOS full adder-subtractor. The output waveform is free from neither degradation problem nor propagation delay problem. However, noises can been seen in the output waveform where spikes are occurred in output waveform. This circuit consumed 112.81 μm power with 279.77×10^{-16} J of power-delay product. Figure 9 shows the layout of the 4 bit full adder-subtractor of this design. The area of the layout is 42.550×19.500 μm (829.725 μm^2).

The third, design approach is to cascade four 1 bit pass transistor logic full adder-subtractor with PTL gate XOR gate as the signal control circuit inside each full adder-subtractor block. The output waveform is free from degradation problem but experienced propagation delay problem caused by the buffer gate used in each building block. Voltage spikes are formed under the problem and became a source of unwanted noises to the circuit. The circuit consumed 133.34 μm power with 361.35×10^{-16} J of power-delay product. Figure 10 shows the layout of the 4 bit full adder-subtractor of third design approach. The area of the layout is 29.720×16.140 μm (479.681 μm^2).

Forth, design approach is to cascade four 1 bit transmission gate full adder-subtractor with transmission gate XOR gate as the signal control circuit inside each full adder-subtractor block. The FAS operate with the full output voltage swing however, there are few voltage spikes that can be seen in the output waveform of the circuit that caused by the current leakage due the instantaneous delay during the interchange of state of input signals. This circuit consumed 139.40 and 361.05×0^{-16} J of power-delay product. Figure 11 shows the layout of the 4 bit full adder-subtractor of fourth design approach. The area of the layout is 38.620×17.650 μm (681.643 μm^2).

Table 1 shows the comparison of 4 bit full adder-subtractor of each design approaches. Buffered PTL approach has the lowest transistor count of 104 transistors where it is <27.78% the static CMOS approaches however, 4 bit full adder-subtractor composed by static CMOS full adder with TG XOR has the lowest power consumption and lowest power-delay product with are 112.81 μW and 279.77×10^{-16} J, respectively. The difference of these two values with the highest values of other approaches are 19.0 and 36.98%, respectively. PTL logic approach clearly shown that it has the lowest area occupied which is 479.681 μm^2 or 37.78%l ower than the static CMOS approach. Generally, pass transistor logic approach in designing the full adder-subtractor shows the highest potential which meet the low area, low power

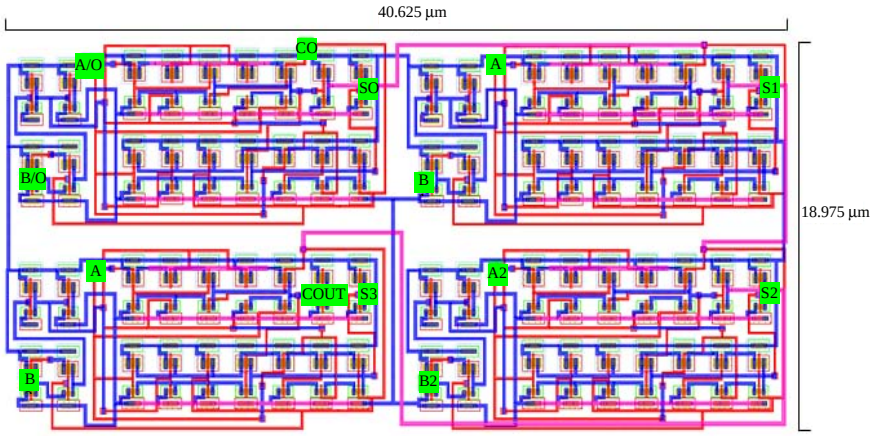

Fig. 8: Layout diagram of 4 bit static CMOP FAS with PTL XOR

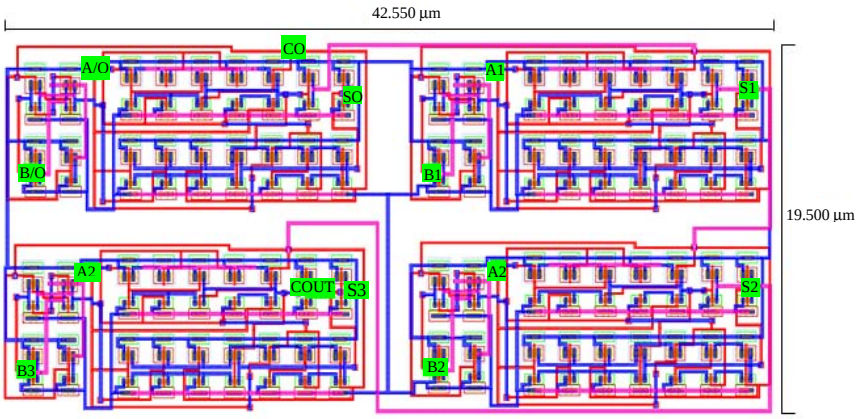

Fig. 9: Layout diagram of 4 bit static CMOP FAS with PTL XOR

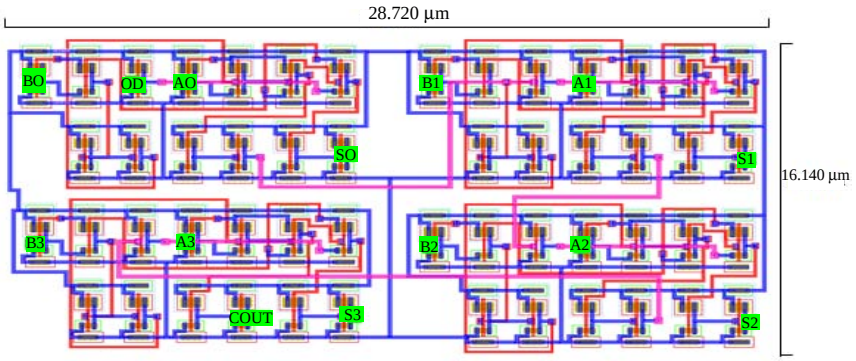

Fig. 10: Layout diagram of 4 bit PTL FAS

consumption and high performance requirements in term of power-delay product. However, due to the degrade problem in PTL, one or more buffer gate are used to amplified the output signal to resolve the problem.

Whenever signals passing through the buffer gates, high propagation delay is happened and affects the power consumption and power-delay product of the PTL approaches. Transmission gate approach is tended to synthesis the degradation problem in PTL but results in

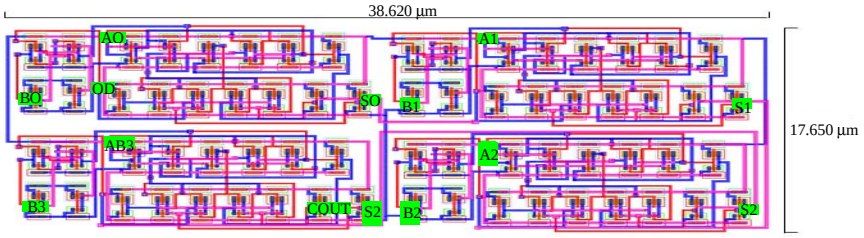

Fig. 11: Layout diagram of 4 bit TG FAS

Table 1: Comparison of 4 bit full adder-subtractor

Design	Transistor count	Average delay (Psec)	Power consumption (µW)	Power delayp product ($\times 10^{-16}$ J)	Area (µm^2)
Static CMOS+PTL	144	323	137.45	443.96	770.859
Static CMOS+TG	144	248	112.81	279.77	829.725
Buffered PTL	104	271	133.34	361.35	479.681
TG	136	259	139.40	361.05	681.643

higher transistor count and higher area occupied. Apart from the conventional static CMOS approach, both PTL and TG approaches are able to conclude that have high potential in present VLSI design trend by using proper method to solve the degradation and propagation delay problem.

CONCLUSION

Conclusion, it shows that the transistor count of proposed pass transistor approach and transmission gate approach is lesser compared to conventional static CMOS technology and thus the size of the integrated circuit can be reduced. However, the power consumption and power-delay product of the circuit does not meets the expectation due to the natural behaviour of pass transistor logic which caused some significant instantaneous delay and leaded toward a high power consumption and high power-delay product. Nevertheless, pass transistor logic and transmission logic are highly potential in integrated circuit design as these two approaches are able to reduce the overall transistor count with proper synthesis in resolving their problems.

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