Journal of Engineering and Applied Sciences 12 (11): 2984-2989, 2017
ISSN: 1816-949X

Reversible Realization of Common Bus Structure for ALU Applications

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Abstract: Growth of research in the field of effective digital computing systems leads to the need of efficient digital design approaches. Reversible logic concept is the result of this necessity. This design approach creates low power efficient digital circuits with improved performance. In the CPU/ALU bus provides the path for data flow and covers major area of the CPU. As the conventional buses are irreversible in nature when data flows through these buses it consumes power and additional hardware is required to sink the generated heat. Moreover by designing a bus using reversible technology power requirement is decreased with the removal of need of heat sink. In this study, we focus upon the designing of common bus structure using reversible logic approach. Common bus structure provides an effective way to provide the facility of communication between computer subsystems. The proposed approach for reversible realization of common bus system is simulated and synthesized for ModelSim simulator and Xilinx Software, respectively.

Key words: Common bus structure, VSMT gate, Sayem gate, reversible realization of digital circuits, nature, apporach

INTRODUCTION

Digital computing systems have various sub systems which coordinate and communicate for the generations of required results. Common bus is the solution to this requirement. It provides an efficient scheme of information transfer between various registers in a computer system. Generally, common bus structure is designed using multiplexer circuits to connect registers requiring communication of data bits.

Earlier any digital circuit was designed using AOI design approach. AOI approach utilised available digital logic gates such AND OR and NOT gates to design digital circuits and systems. These digital logic gates may be referred to as conventional digital logic gates. These conventional logic gates have n input signals and a single output signal (generally n>1). So, these conventional digital logic gates tend to cause loss of information after the operation. This loss of information is the main cause of heat loss from any digital computing system.

In the year 1961, Landauder has given the formula kTln 2 joules to calculate the energy loss per bit loss. This leads to the calculation of generated heat from the digital system (Landaure, 1961). Later in the year 1970 G.E. Moore has proposed that component density for unit chip area increases by approximately 2 times in every 18 month's time span as shown in Fig. 1 (Moore, 1965).

This increase in component density leads to the increase in the amount of heat generation exponentially. This phenomenon leads to the degeneration of performance and efficiency of the digital systems.

After that in year 1973, C.H. Bennett has proposed that the process of heat generation from any digital system can be removed or reduced by redesigning the digital circuits with reversible logic approach (Bennett, 1973). This method ideally creates lossless digital circuits and systems. Reversible logic concept aims to design any target digital system using reversible design entities only. Here basic design entities are reversible logic gates only. Various digital circuits have been already designed using these reversible logic gates with reduced heat generation and improved performance. In this study, we have proposed a design approach for the reversible realization of common bus architecture.

Common bus structure: Any computer system performs different operations with the help of arithmetic logic unit. Various sub systems of a computer system have a need of communication with each other for performing desired operation. Common bus system is the most suitable solution for this communication requirement problem (Fletcher, 1980; Floyd, 2006; Mano, 1979). Various

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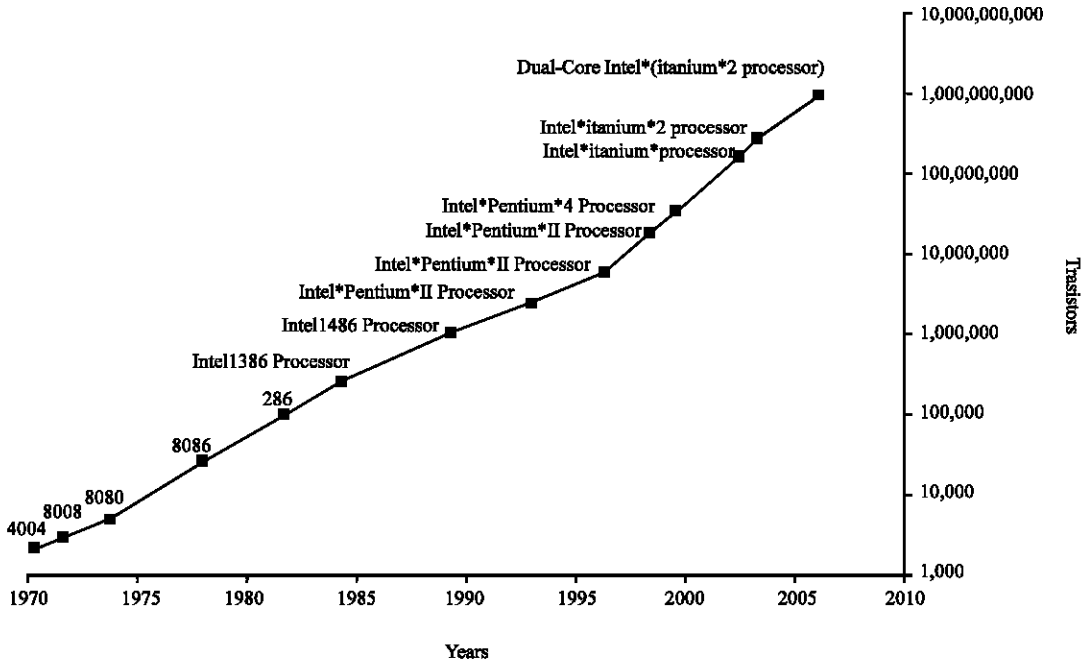

Fig. 1: Moore's Law

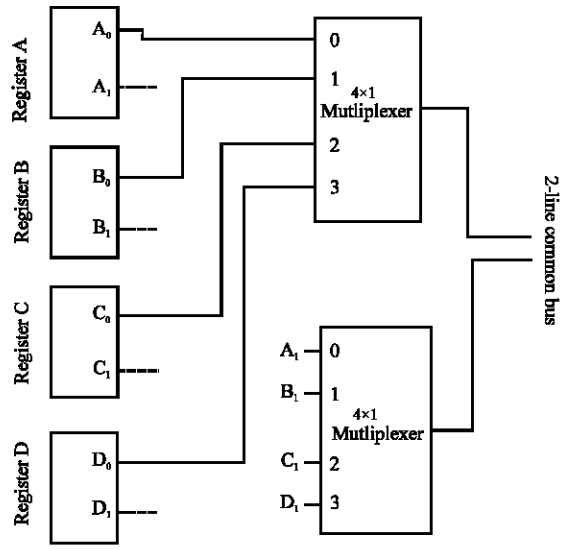

Fig. 2: Common bus structure

subsystems in a computer system are connected through common bus structure. Generally common bus is designed using multiplexer circuit as shown in Fig. 2.

This Fig. 2 shows that the common bus is a connection for four 2 bit registers here. Similarly other subsystems may also be connected through common bus. Here depending upon the combinations of the selection line applied source register is selected whose binary data is transferred on the bus. After that the destination register is selected which receives the data from the common bus.

Total number of multiplexers required in the common bus is actually derived by the size of the data communicated whereas number of selection lines for multiplexers depend upon the total number of subsystems connected through the common bus.

Fundamentals of reversible realization of digital circuits: Reversible realization of any digital circuit basically targets to redesign the circuits with various reversible units for generating low loss efficient digital systems (Thapliyal and Srinivas, 2005a, b; Wang *et al*., 2012; Haghparast and Navi, 2007; Hv *et al*., 2012). Some fundamentals description of terms related with reversible logic approach are as follows.

Reversible logic gates: These are digital logic gates with equal number of input and output signals (Saravanan and Manic, 2013; Toffoli, 1980; Fredkin and Toffoli, 1982). Information regarding the applied inputs signals may be generated at any instant by knowing the generated output signals due to one-to-one mapping between input and output signals. Some examples of reversible logicgates are Feynman, Toffoli, Fredkin, Peres, TKS, Sayem and VSMT gates, etc. (Feynman, 1985; Peres, 1985; Thapliyal and Srinivas, 2005a, b; Kamani *et al*., 2015; Shukla *et al*., 2014; Haghparast and Navi, 2008). Figure 3 shows some examples of reversible logic gates with some descriptions.

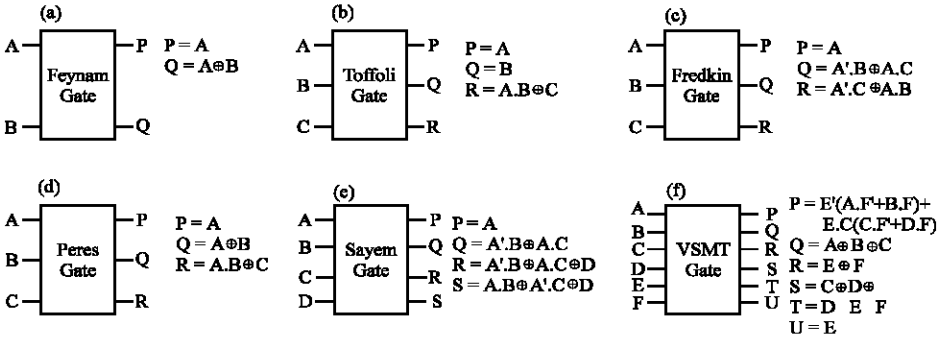

Fig. 3: Examples of reversible logic gates; block diagram and output equations of: a) Feynam gate; b) Toffoli gate; c) Fredkin gate; d) Peres gate; e) sayem gate and f) VSMT gate

Performance parameters: In reversible design approach researchers have to consider the requirement of optimization of some performance parameters (Thapliyal and Ranganathan, 2009; Shukla *et al*., 2016a, b; Ni *et al*., 2010; Ali *et al*., 2011). Some of these performance parameters are as follows.

Total reversibile logic gates: It is defined as the total number of reversible logic gates utilised in designing the digital circuit using reversible design approach. Ideally single reversible logic gate should be used to design any digital circuit (Shukla *et al*., 2015a-c; Haghparast *et al*., 2011; Syamala and Tilak, 2011). Although, minimum reversible logic gates are aimed by reversible circuit designers.

Constant input signals: Constant input signals are additional high or low input signals required to be applied to complete the working of the designed reversible circuits (Sengupta *et al*., 2011; Thunuguntla *et al*., 2012; Shukla *et al*., 2015a-c). These signals are actually overhead signals required for the design, so are considered as adversely affecting performance parameters. Thus, this performance parameter is also minimized by the reversible circuit designers. Ideally zero constant inputs should be applied to the designed reversible circuit.

Garbage output signals: These are defined as additional output signals generated from the designed reversible circuit apart from the desired output signals (Thapliyal and Vinod, 2007; Nagamani *et al*., 2011; Shukla *et al*., 2016a, b). These signals tend to increase the amount of heat generation from the designed reversible circuits, thus are required to be minimized by the researchers. Ideally no garbage output signal should be generated from the designed reversible circuit.

Increase in the garbage output signals leads to degrade the required performance of the designed reversible circuit.

Quantum cost: Quantum cost of any reversible design is generated by calculating quantum cost of basic (1×1 and 2×2 size) reversible logic gates (Thapliyal *et al*., 2013; Frank, 2005; Sayem and Ueda, 2010). Calculation of quantum cost of reversible design is calculated by taking cost of 1×1 size logic gates equals to zero whereas 2×2 size gate as one. This parameter is also minimized by the reversible circuit designers to enhance the performance of the reversible design.

These parameters are optimized to improve the performance and efficiency of digital reversible circuits and systems. Till now various reversible designs have been already proposed by reversible circuit designers (Mahfuzzreza *et al*., 2013). Optimized designs for different designs are being also presented by the researchers with improved performance parameters measures. It includes reversible realization of various combinational and sequential digital circuits along with storage circuits and systems.

Reversible realization of digital circuits: In this approach, various reversible logic gates are used to design the aimed digital circuit (Guan *et al*., 2011; Shukla *et al*., 2015a, b). Designed reversible circuits are planned with optimized performance parameters. An ideal reversible design should have following performance parameters:

- Single reversible logic gate required
- No constant input signal applied
- Zero garbage output signals generated
- No feedback connection in the design
- Low quantum cost

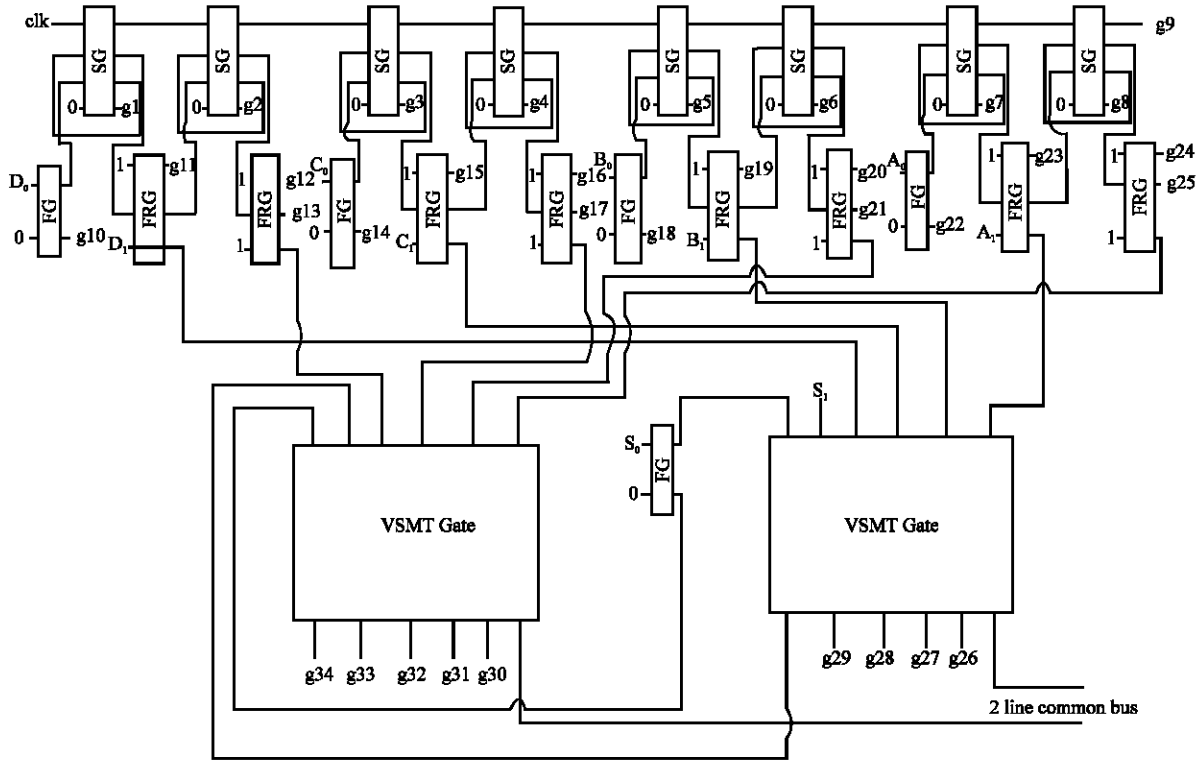

Fig. 4: Proposed design

Table 1: Selection of registers through common bus

	Selection lines	
Selected register	S_0	S_1
A	0	0
B	1	0
C	0	1
D	1	1

MATERIALS AND METHODS

Proposed design: We propose a common bus structure to connect four registers of 2 bits each. As shown in Fig. 4, four 2 bits registers A, B, C, D are connected through common bus using multiplexers only. In our proposed design approach for reversible realization of common bus circuit, registers are designed using Feynman, Fredkin and Sayem gates whereas multiplexer circuits are designed using VSMT gates only.

Here two selection lines S_1 and S_0 are applied in VSMT gates to select any of the desired register out of four connected registers A, B, C, D as shown in Table 1. As shown in Table 1, combination of selection inputs applied to the multiplexer circuits will select the desired registers and its signals will be transferred to the bus line.

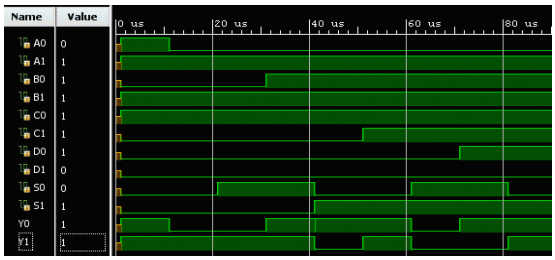

Fig. 5: Simulated waveform of the proposed design

RESULTS AND DISCUSSION

Simulation and result analysis: Proposed design for the reversible realization of common bus structure is Fig. 5. Simulated waveform of the proposed designsynthesized and simulated for Xilnx software and ModelSim simulator respectively. Simulation result for proposed design is shown in Fig. 5. It clearly conforms to the desired working of the common bus as mentioned in Table 1.

As no earlier designs are proposed for the reversible realization of common bus structure this approach may be considered as the first approach for the same. In the proposed design, total number of reversible logic gates used is 23 which generate a total of 34 garbage output signals.

CONCLUSION

Various subsystems of a computer ALU require a medium of communication for proper functioning and to generate required results. Simple wires are replaced by common bus structure to provide an efficient scheme of communication in this regard. Generally multiplexer circuits are used to design common bus to connect various subsystems. In this study, we have proposed an approach for reversible realization of common bus structure to connect four 2 bit registers. This design utilizes 23 reversible logic gates and generates a total of 34 garbage output signals. Proposed design is simulated with ModelSim simulator. Simulated waveform of proposed circuit conforms to the desired working of the common bus. The proposed design may be further optimized and utilized for designing low loss high performance digital systems.

ACKNOWLEDGEMENTS

The researchers are thankful to Mr. Aseem Chauhan (Additional President RBEF, Chancellor AUR), Maj. General K. K. Ohri, AVSM (Retd.), Pro. Vice Chancellor, AUUP, Lucknow Campus, Wg Cd (Dr) Anil Kumar (Director, ASET) for their cooperation, motivation and suggestive guidance.

REFERENCES

Ali, M.B., H.A. Rahman and M.M. Rahman, 2011. Design of a high performance reversible multiplier. Intl. J. Comput. Sci., 8: 134-141.

Bennet, C.H., 1973. Logical reversibility of computation. IBM J. Res. Dev., 17: 525-532.

Feynman, R., 1985. Quantum mechanical computers. Optics News, 11: 11-20.

Fletcher, W.I., 1980. An Engineering Approach to Digital Design. Prentice-Hall, Upper Saddle River, New Jersey, ISBN:9780132776998, Pages: 766.

Floyd, T.L., 2006. Digital Fundamentals. 9th Edn., Pearson Prentice Hall, New York, USA., ISBN-13: 9780131946095, Pages: 871.

Frank, M.P., 2005. Introduction to reversible computing: Motivation, progress and challenges. Proceedings of the 2nd Conference on Computing Frontiers, May 04-06, 2005, ACM, Ischia, Italy, ISBN:1-59593-019-1, pp: 385-390.

Fredkin, E. and T. Toffoli, 1982. Conservative logic. Int. J. Theor. Phys., 21: 219-253.

Guan, Z., W. Li, W. Ding, Y. Hang and L. Ni, 2011. An arithmetic logic unit design based on reversible logic gates. Proceedings of the 2011 IEEE Pacific Rim Conference on Communications Computers and Signal Processing (PacRim), August 23-26, 2011, IEEE, Victoria, British Columbia, Canada, ISBN:978-1-4577-0252-5, pp: 925-931.

Haghparast, M. and K. Navi, 2007. A novel reversible full adder circuit for nanotechnology based systems. J. Applied Sci., 7: 3995-4000.

Haghparast, M. and K. Navi, 2008. A novel fault tolerant reversible gate for nanotechnology based systems. Am. J. Applied Sci., 5: 519-523.

Haghparast, M., M. Hajizadeh, R. Hajizadeh and R. Bashiri, 2011. On the synthesis of different nanometric reversible converters. Middle-East J. Sci. Res., 7: 715-720.

Hv, R.A., R. Chinmaye and K.N. Muralidhara, 2012. Design, optimization and synthesis of efficient reversible logic binary decoder. Intl. J. Comput. Appl., 46: 45-51.

Kamani, K., S. Koneti and U. Bollampalli, 2014. Energy efficient reversible logic design for code converters. ICETET. Intl. J. Res. Appl., 1: 132-136.

Landauer, R., 1961. Irreversibility and heat generation in the computing process. IBM J. Res. Dev., 5: 183-191.

Mahfuzzreza, M., R. Islam and M.B. Ali, 2013. Optimized design of high performance reversible multiplier using BME and MHNG reversible gate. Am. Intl. J. Res. Sci. Technol. Eng. Math., 2: 227-232.

Mano, M.M., 1979. Digital Logic and Computer Design. Prentice Hall, New York, USA., ISBN-13: 9780132145107, Pages: 612.

Moore, G.E., 1965. Cramming more compounds onto integrated circuits. Moore's Law Publishing, Cambridge, Massachusetts.https://cseweb.ucsd.edu/classes/wi09/cse240c/Slides/02_MooresLawAnd8080.pdf

Nagamani, A.N., H.V. Jayashree and H.R. Bhagyalakshmi, 2011. Novel low power comparator design using reversible logic gates. Indian J. Comput. Sci. Eng., 2: 566-574.

Ni, L., X. Dai, Z. Guan and W. Li, 2010. Using new designed NLG gate for the realization of four-bit reversible numerical comparator. Proceedings of the 2010 International Conference on Educational and Network Technology (ICENT), June 25-27, 2010, IEEE, Qinhuangdao, China, ISBN:978-1-4244-7660-2, pp: 254-258.

Peres, A., 1985. Reversible logic and quantum computers. Phys. Rev. A, 32: 3266-3276.

Saravanan, M. and K.S. Manic, 2013. Energy efficient code converters using reversible logic gates. Proceedings of the 2013 IEEE International Conference on Green High Performance Computing (ICGHPC), March 14-15, 2013, IEEE, Nagercoil, India, ISBN:978-1-4673-2592-9, pp: 1-6.

Sayem, A.S.M. and M. Ueda, 2010. Optimization of reversible sequential circuits. J. Comput., 2: 208-214.

Sengupta, D., M. Sultana and A. Chaudhuri, 2011. Realization of a novel reversible SCG gate and its application for designing parallel adder: Subtractor and match logic. Intl. J. Comput. Appl., 31: 30-35.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2014. A novel approach to design decimal to BCD encoder with reversible logic. Proceedings of the 2014 International Conference on Power Control and Embedded Systems (ICPCES), December 26-28, 2014, IEEE, Allahabad, India, ISBN:978-1-4799-5913-6, pp: 1-5.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2015c. A novel approach to design a 4-Bit binary comparator circuit with reversible logic using CDSM gate. Intl. J. Bus. Data Commun. Netw., 11: 36-49.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2015a. A novel approach to design a redundant binary signed digit adder cell using reversible logic gates. Proceedings of the 2015 IEEE UP Section Conference on Electrical Computer and Electronics (UPCON), December 4-6, 2015, IEEE, Allahabad, India, ISBN:978-1-4673-8506-0, pp: 1-6.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2015b. Application of CSMT gate for efficient reversible realization of binary to gray code converter circuit. Proceedings of the 2015 IEEE UP Section Conference on Electrical Computer and Electronics (UPCON), December 4-6, 2015, IEEE, Allahabad, India, ISBN:978-1-4673-8507-7, pp: 1-6.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2016a. A novel approach for reversible realization of 8-bit adder-subtractor circuit with optimized quantum cost. Proceedings of the International Conference on Emerging Trends in Engineering Technology and Science (ICETETS), February 24-26, 2016, IEEE, Pudukkottai, India, ISBN:978-1-4673-6726-4, pp: 1-6.

Shukla, V., O.P. Singh, G.R. Mishra and R.K. Tiwari, 2016b. An efficient approach for reversible realization of 1:4 demultiplexer circuit. Proceedings of the International Conference on Emerging Trends in Electrical Electronics & Sustainable Energy Systems (ICETEESES), March 11-12, 2016, IEEE, Sultanpur, India, ISBN:978-1-5090-2119-2, pp: 229-233.

Syamala, Y. and A.V.N. Tilak, 2011. Reversible arithmetic logic unit. Proceedings of the 3rd International Conference on Electronics Computer Technology (ICECT) 2011 Vol. 5, April 8-10, 2011, IEEE, Kanyakumari, India, ISBN:978-1-4244-8678-6, pp: 207-211.

Thapliyal, H. and A.P. Vinod, 2007. Design of reversible sequential elements with feasibility of transistor implementation. Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2007), May 27-30, 2007, IEEE, New Orleans, Louisiana, ISBN:1-4244-0920-9, pp: 625-628.

Thapliyal, H. and M.B. Srinivas, 2005a. A new reversible TSG gate and its application for designing efficient adder circuits. Proceedings of the 7th International Symposium on Representations and Methodology of Future Computing Technologies (RM 2005), September 5-6, 2005, Cornell University, Tokyo, Japan, pp: 1-5.

Thapliyal, H. and M.B. Srinivas, 2005b. Novel design and reversible logic synthesis of multiplexer based full adder and multipliers. Proceedings of the 48th Midwest Symposium on Circuits and Systems, Volume 2, August 7-10, 2005, Covington, USA., pp: 1593-1596.

Thapliyal, H. and N. Ranganathan, 2009. Design of efficient reversible binary subtractors based on a new reversible gate. Proceedings of the Annual Symposium on Computer Society, May 13-15, 2009, Tampa, FL., pp: 229-234.

Thapliyal, H., N. Ranganathan and S. Kotiyal, 2013. Design of testable reversible sequential circuits. IEEE. Trans. Very Large Scale Integr. Syst., 21: 1201-1209.

Thunuguntla, L., K.B. Madhavi and T. Pullaiah, 2012. Designing of efficient online testable reversible multiplexers and demultiplexers with new reversible gate. Intl. J. Eng. Res. Appl., 2: 183-191.

Toffoli, T., 1980. Reversible computing, tech memo MIT/LCS/ TM-151. MIT Computer Science and Artificial Intelligence Laboratory, Cambridge, Massachusetts.

Wang, J.C., Y. Pang and Y. Xia, 2012. A BCD priority encoder designed by reversible logic. Proceedings of the 2012 International Conference on Wavelet Active Media Technology and Information Processing (ICWAMTIP), December 17-19, 2012, IEEE, Chengdu, China, ISBN:978-1-4673-4684-9, pp: 318-321.