Journal of Engineering and Applied Sciences 11 (7): 1687-1692, 2016
ISSN: 1816-949X

A Design of the DC Offset Error Compensator with Prompt Response to the Grid Voltage in PLL

Chang Seok Park and Tae Uk Jung
Department of Electrical Engineering, Kyungnam University,
Changwon, Republic of Korea

Abstract: This study proposes the dc offset error compensation algorithm using d-q synchronous coordinate transform Phase-Locked-Loop (PLL) in single-phase grid-connected converters. The dc offset errors are caused by the process of analog to digital conversion and the distorted grid voltage. These errors must be resolved because the dc offset error should generate the estimated grid frequency error of the PLL. In conventional algorithm to compensate the DC offset, the DC offset is estimated by integrating the synchronous reference frame d-axis voltage during one period of the grid voltage. The existing algorithm has a drawback that is a slow dynamic response because monitoring the one period of the grid voltage is required. The proposed algorithm has a prompt dynamic response because the DC offset is continuously estimated by transforming the d-axis voltage to synchronous reference frame without monitoring one cycle time of the grid voltage. The proposed algorithm is verified by PSIM simulation and the experimental test.

Key words: DC offset error, compensator, PLL, single-phase grid-connected converter, coordinate transformation

INTRODUCTION

Coal, oil and other fossil energy resources become increasingly deficient and greenhouse gas emissions bring about a large number of environmental pollution problems. Therefore, recently research on renewable energy sources has been focused worldwide (Tipsuwanporn *et al*., 2011; Infield *et al*., 2004; Benjanarasut and Neammanee, 2011).

The Single-phase Grid-connected Converter (SGC) is very important for the renewable energy conversion systems such as photovoltaic wind power and fuel cells in home and industrial appliances (Wang *et al*., 2010). The PLL method for the power quality, system efficiency and reliability in the SGC system is one of the important factors (Saitou *et al*., 2003). However, the PLL is seriously influenced by the sensing operation of the Analog to Digital Conversion (ADC) and the distorted grid voltage. Because of these effects, the DC offset errors of the PLL should be generated.

If the DC offset error is included in the PLL system, it can cause distortion in the grid angle estimation with PLL. Accordingly, recent study has dealt with the integral technique using the Synchronous Reference Frame (SRF) method (Cai *et al*., 2013; Golestan *et al*., 2015; Ohkubo and Kobayashi, 2008). This algorithm has advantage which is not required any additional hardware and can be implemented by a simple proportional-integral controller and an integral operation. However, the existing algorithm has a drawback that is a slow dynamic response because monitoring the one period of the grid voltage is required (Hwang *et al*., 2012; Li *et al*., 2014). The proposed dc offset error compensation algorithm has a prompt dynamic response because the dc offset error is continuously estimated by transforming the d-axis voltage to SRF without monitoring one cycle time of the grid voltage.

MATERIALS AND METHODS

System modeling

DC offset error generation: Figure 1 shows the system configuration of the SGC including power circuits and control algorithm based on d-q SRF method. Figure 2 describes the block diagram of a basic single-phase grid-connect PLL based on d-q SRF method. The single-phase grid-connect PLL system is implemented by generating virtual voltage which is delayed by 90° from the grid voltage and it can be achieved by using digital All Pass Filter (APF) as shown in Fig. 2. The measured grid voltage V_{grid} is set to be V_{ds} and V_{qs} is the virtual voltage though the APF. V_{ds} and V_{qs} are converted to V_{ds} and V_{qs} in the d-q SRF method. The ideal grid voltage can be calculated by Eq. 1:

Corresponding Author: Chang Seok Park, Department of Electrical Engineering, Kyungnam University, Changwon, Republic of Korea

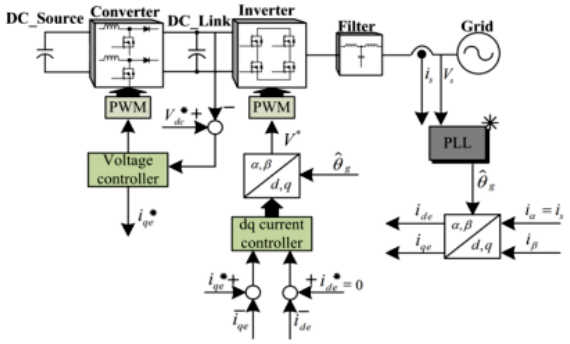

Fig. 1: Conrrol block diagram of single-phase grid-connected converters

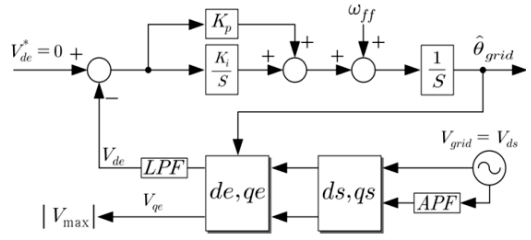

Fig. 2: Structure of d-q SRF method in PLL

$$V_{ds} = -V_m \sin \omega_g t \tag{1}$$

Where:
V_m = The grid voltage peak value
ω_g = The grid angular frequency respectively

In order to obtain the estimated grid angle, frequency and amplitude, d-q axis voltages are transformed by the d-q synchronous coordinate transformation. The transformation matrix is depended on estimation grid angle. The transformation matrix can be the following Eq. 2:

$$T(\hat{\theta}_g) = \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \tag{2}$$

where, θ_g is the estimated grid angle. Considering, the component V_{ds} can be written as:

$$V_{ds} = -V_m \sin(\theta_g - \hat{\theta}g) \tag{3}$$

where,θ_g the real grid angle. The angle difference (θ_g-θ_g) is too small and the PLL output θ_g can track the angle of the grid voltage. However, V_{ds} is included as system clock noise and distorted wave of the real grid voltage. Therefore V_{ds} passing through the d-q synchronous coordinate transform generates the dc offset errors V_{ds_err} including the dc offset error can be rewritten by Eq. 4:

$$V_{ds\_err} = -\Delta_s V_m \sin \omega_g t + \Delta_{off} \tag{4}$$

Where:
Δ_s = The scaling error component
Δ_{err} = The offset error component

Considering the errors, the synchronous d-axis V_{ds_err} and q-axis voltages V_{qs_err} can be obtained as follows Eq. 5:

$$\begin{aligned} \begin{bmatrix} V_{de\_err} \\ V_{qe\_err} \end{bmatrix} &= \begin{bmatrix} V_{ds\_err} \\ V_{qs\_err} \end{bmatrix} \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \\ &= \begin{bmatrix} -\Delta_s V_m \sin\omega_g t + \Delta_{off} \\ \Delta_s V_m \cos\omega_g t + \Delta_{off} \end{bmatrix} \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \end{aligned} \tag{5}$$

In other to obtain the estimated grid angle, frequency and amplitude, synchronous d-axis voltage has to be converged to zero. However, synchronous d-axis voltage may not be able to converge to zero due to Δ_{off}. From Eq. 5, the synchronous dq-axis voltages including the scaling error and the dc offset errors can be calculated by Eq. 6:

$$\begin{bmatrix} V_{de\_err} \\ V_{qe\_err} \end{bmatrix} = \begin{bmatrix} -\Delta_s V_m \sin(\theta_g - \hat{\theta}_g) + \Delta_{off} \cos\hat{\theta}_g + \Delta_{off} \sin\hat{\theta}_g \\ \Delta_s V_m \cos(\theta_g - \hat{\theta}_g) - \Delta_{off} \sin\hat{\theta}_g + \Delta_{off} \cos\hat{\theta}_g \end{bmatrix} \tag{6}$$

If the angle difference (θ_g-θ_g) is too small, the synchronous dq-axis voltages can be rewritten by Eq. 7:

$$\begin{bmatrix} V_{de\_err} \\ V_{qe\_err} \end{bmatrix} = \begin{bmatrix} \Delta_{off} \cos\hat{\theta}_g + \Delta_{off} \sin\hat{\theta}_g \\ \Delta_s V_m - \Delta_{off} \sin\hat{\theta}_g + \Delta_{off} \cos\hat{\theta}_g \end{bmatrix} \tag{7}$$

Therefore, the error values of the converted synchronous dq-axis coordinate can be confirmed that it has a component of the sine and cosine term. Also, the ripple frequency is able to know consists of the grid frequency components. Moreover, the synchronous d-axis voltage does not include the ripple components related to the scaling error as shown in Eq. 7. In other words, the scaling error does not cause the distortion in the estimated grid angle but affects the estimated grid voltage amplitude related to the synchronous q-axis voltage. It only related to the feed-forward term at the output of the current controller. Therefore, the only dc offset error is considered to reduce the distortion of the estimated grid angle in this study.

Proposed compensation algorithm: The dc offset error of synchronous d-axis voltage causes the distorted grid

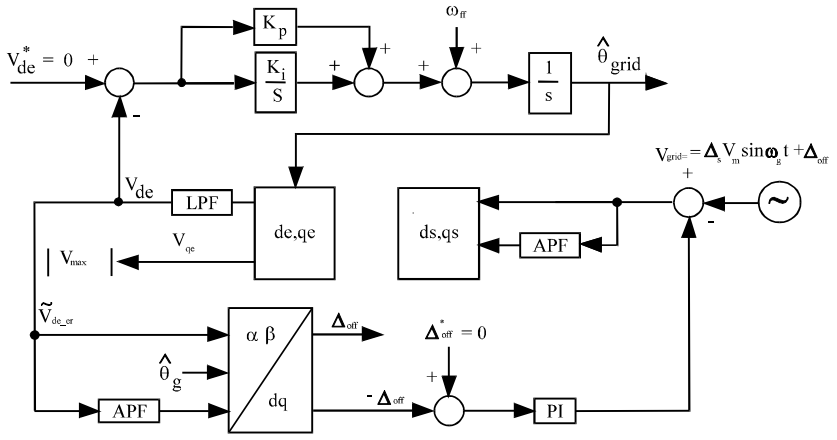

Fig. 3: Proposed offset error compensation algorithm block diagram

angle and grid frequency in the PLL system. The frequency component of the synchronous d-axis voltage is same as the grid frequency. The existing method for the dc offset error value can be estimated by integrator operation of the grid frequency period. As the result, the dc offset error can be compensated by reducing the ripple components of the synchronous d-axis voltage in a PLL. However, the existing integral compensator has a drawback that is a slow dynamic response because monitoring the one period of the grid voltage is required. The proposed algorithm has a prompt dynamic response because the dc offset error is continuously estimated by transforming the d-axis voltage to SRF method without monitoring one cycle time of the grid voltage.

Figure 3 shows the proposed dc offset error compensation algorithm block diagram based on the single-phase grid-connect converters. The synchronous d-axis voltage is directly used for the input signal of the proposed technique. Consequently, the dc offset error value can be easily estimated by the synchronous dq-axis coordinate transformation of the synchronous d-axis voltage including the dc offset error value.

From Eq. 7 V_{de_err} the is composed of the sine and cosine terms whit the dc offset error. Therefore, the dc offset error value is estimated by. The is set to Eq. 8

$$\alpha = V_{de\_err}$$

where, α is sinusoidal wave caused by the dc offset error. The two axes of the α, β are required for the synchronous coordinated conversion. Thus, the virtual voltage β is delay by 90° from the and it can be achieved by using DAPF. The rectangular coordinate system of the α, β can be calculated by Eq. 9:

$$\begin{bmatrix}\alpha\\ \beta\end{bmatrix} = \begin{bmatrix}\Delta_{off}\cos\hat{\theta}_g + \Delta_{off}\sin\hat{\theta}_g\\ \Delta_{off}\sin\hat{\theta}_g - \Delta_{off}\cos\hat{\theta}_g\end{bmatrix} \quad (9)$$

Considering Eq. 2 and 9 the synchronous coordinated system can be written as Eq. 10:

$$\begin{aligned}\begin{bmatrix}V_{de\_off}\\ V_{qe\_off}\end{bmatrix} &= \begin{bmatrix}\alpha\\ \beta\end{bmatrix}\begin{bmatrix}\cos\hat{\theta}_g & \sin\hat{\theta}_g\\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g\end{bmatrix}\\ &= \begin{bmatrix}\Delta_{off}\cos\hat{\theta}_g + \Delta_{off}\sin\hat{\theta}_g\\ \Delta_{off}\sin\hat{\theta}_g - \Delta_{off}\cos\hat{\theta}_g\end{bmatrix}\begin{bmatrix}\cos\hat{\theta}_g & \sin\hat{\theta}_g\\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g\end{bmatrix}\\ &= \begin{bmatrix}\Delta_{off}\\ -\Delta_{off}\end{bmatrix}\end{aligned} \quad (10)$$

The proposed compensator consists of two parts as shown in Fig. 3. The first part is the dq-axis coordinated transformation system used for estimating the dc offset error. The other is the Proportional-Integral (PI) controller to decrease the dc offset error value. In addition, the output of the proposed PI controller is updated to get the constant of the exact dc offset error value in real time.

RESULTS AND DISCUSSION

Figure 4 shows the simulation circuit for the SGP using the PSIM simulator. The rated power is designed as 3 kW. The parameter of SPC is displayed in Table 1.

Figure 5 displays the simulation results considering the dc offset error of 10. Figure 5, the synchronous d-axis voltage has the same ripples with the grid frequency.

Figure 6a, b show the waveform comparing the dynamic characteristics of the proposed method and the existing method under 10 dc offset error. Figure 6a presents the waveform that is compensated error in the

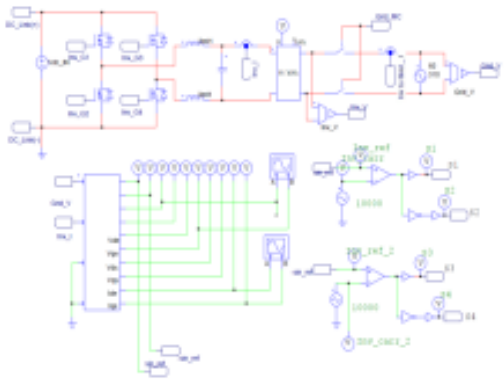

Fig. 4: Simulation circuit of the SGP

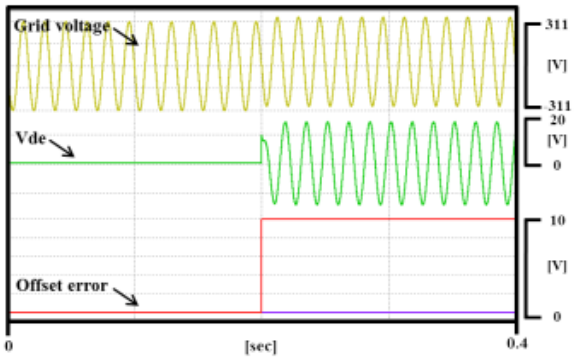

Fig. 5: Waveform after injecting the dc offset error 10 V of the grid voltage

existing integral method, the dc offset error compensation time is 180 msec. Figure 6b illustrates the waveform that is compensated error in the proposed method, the dc offset error compensation time is 60 msec. The response characteristic of the proposed method is faster than the conventional method because the conventional method is required one period of the grid voltage. In addition, the proposed method is possible to estimate in real time because it is using the coordinate transform.

Figure 7 displays the dc offset error compensation performance of the proposed algorithm. When applied to 10 dc offset error in the grid voltage at 1 sec, the pulsation is seriously generated in maintained the constant synchronous d-axis voltage. The proposed algorithm is immediately started the dc offset error compensation in real time when 2 sec. At this time, the pulsation of the synchronous d-axis voltage is reduced because of the compensation values and the dc offset error values the same. The dc offset error value is changed to 15-3 sec. Finally, the DC offset error value is reduced to 0 V when 4 sec. Although, changing the dc offset error value, the pulsation of the synchronous d-axis voltage is

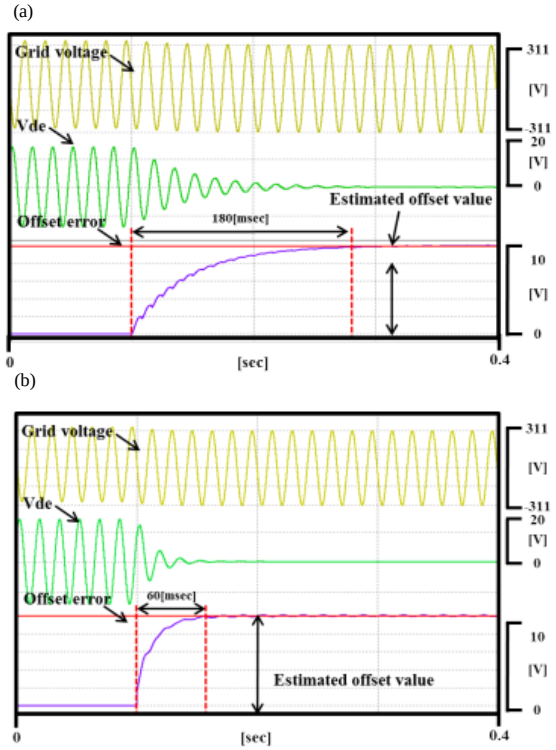

Fig. 6: Comparison of the simulation results with the conventional method; a) Compensation waveform by the conventional method at 10 V DC offset error of the grid voltage; b) Compensation waveform by the proposed method at 10 V DC offset error of the grid voltage

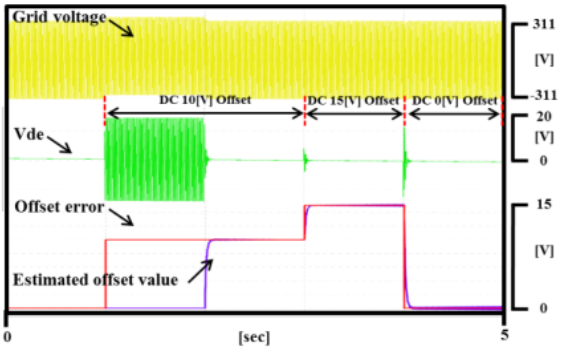

Fig. 7: Waveform according to changing the DC offset error

quickly deleted because the dc offset error value is immediately estimated. The proposed dc offset error compensation method of synchronous d-axis voltage has been verified on a 3 kWSGC. This converter is designed based on the 32 bit DSP control system operating at 10 kHz. The prototype of a 3 kW SGC is shown in Fig. 8.

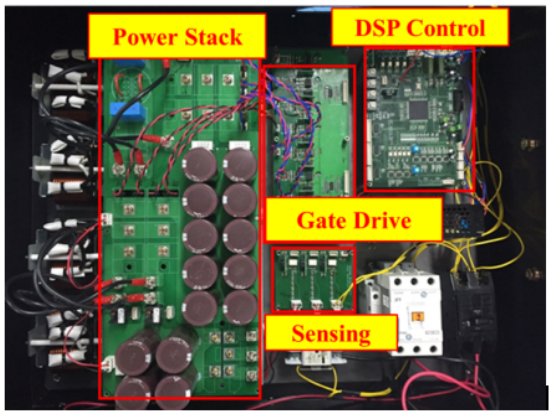

Fig. 8: Prototype of a 3 kW single-phase grid-connected converter

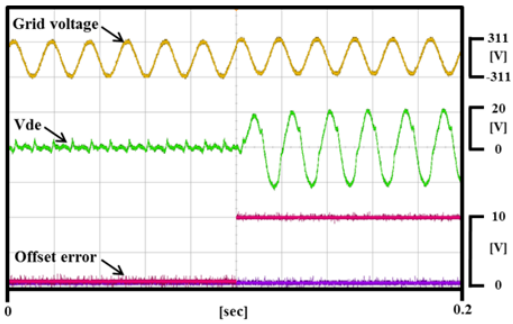

Fig. 9: Experimental results under 10 V dc offset error of the grid voltage

Table 1: The properties of the simulation parameter

Properties	Details
Rated power	3 kW
Switching frequency	16 kHz
Grid voltage	220 Vrms
Grid frequency	60 Hz
DC Link voltage	370 V
Simulation time step	1 usec

Figure 9 shows the experimental results considering the variation of 10 V DC offset error. After the dc offset error is injected, the pulsation of the synchronous d-axis voltage is generated like simulation results of the figure. The ripple component of the synchronous d-axis voltages is perfectly removed by the proposed compensation method as shown in Fig. 10a presents experimental results of the existing integral method, the dc offset error compensation time is 300 msec. Figure 10b illustrates experimental results of the proposed method, the DC offset error compensation time is 150 msec. Figure 11 displays the DC offset error compensation performance of the proposed algorithm. The experimental conditions are the same as the simulation.

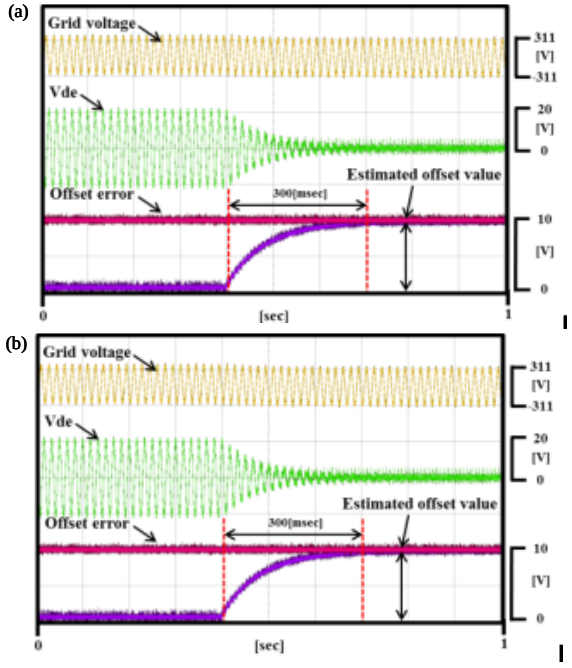

Fig. 10: Comparison of the experimental results with the conventional method (a) Compensation waveform by the conventional method at 10 V dc offset error of the grid voltage (b) Compensation waveform by the proposed method at 10 V DC offset error of the grid voltage

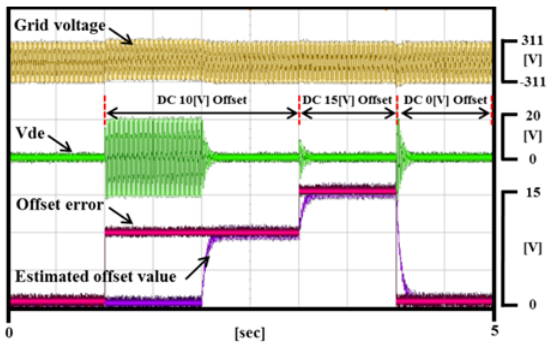

Fig. 11: Waveform according to changing the DC offset error

CONCLUSION

A new dc offset error compensation algorithm for the synchronous reference frame PLL of the single-phase grid-connected converter systems is proposed. The synchronous d-axis voltage is directly used for the input signal of the proposed compensator to detect the dc offset error. As the result, the proposed algorithm has a prompt dynamic response because the DC offset is

continuously estimated by transforming the d-axis voltage to synchronous reference frame without monitoring one cycle time of the grid voltage. The proposed algorithm is utilized without additional hardware. The effect of the proposed algorithm is verified through the several experimental tests. Thus, the proposed method is useful by miniaturizing and reducing the weight for the technical development of a better power conversion device.

REFERENCES

Benjanarasut, J. and B. Neammanee, 2011. The d-, q-axis control technique of single phase grid connected converter for wind turbines with MPPT and anti-islanding protection. Proceeding of the 8th International Conference on Electrical Engineering-Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), May 17-19, 2011, IEEE, Bangkok, Thailand, ISBN:978-1-4577-0425-3, pp: 649-652.

Cai, J., Q.C. Zhong and Z. Deng, 2013. Estimation of srm rotor position based on coordinate transformation. Proceeding of the IEEE 2013-39th Annual Conference on Industrial Electronics Society (IECON), November, 10-13, 2013, IEEE, Sheffield, England, ISBN:978-1-4799-0224-8, pp: 2786-2791.

Golestan, S., M. Ramezani, J.M. Guerrero and M. Monfared, 2015. Dq-frame cascaded delayed signal cancellation-based PLL: Analysis, design and comparison with moving average filter-based PLL. IEEE. Trans. Power Electron., 30: 1618-1632.

Hwang, S.H., L. Liu, H. Li and J.M. Kim, 2012. DC offset error compensation for synchronous reference frame PLL in single-phase grid-connected converters. IEEE. Trans. Power Electron., 27: 3467-3471.

Infield, D.G., P. Onions, A.D. Simmons and G.A. Smith, 2004. Power quality from multiple grid-connected single-phase inverters. IEEE. Trans. Power Delivery, 19: 1983-1989.

Li, J., J. Zhao, J. Wu and P.P. Xu, 2014. Improved dual second-order generalized integrator PLL for grid synchronization under non-ideal grid voltages including DC offset. Proceeding of the 2014 International conference on IEEE Energy Conversion Congress and Exposition (ECCE), September 14-18, 2014, IEEE, Shanghai, China, ISBN:978-1-4799-5776-7, pp: 136-141.

Ohkubo, T. and K. Kobayashi, 2008. A color compensation vision system for color-blind people. Proceedings of the Conference on SICE Annual Conference, August 20-22, 2008, IEEE, Tokyo, Japan, ISBN:978-4-907764-30-2, pp: 1286-1289.

Saitou, M., N. Matsui and T. Shimizu, 2003. A control strategy of single-phase active filter using a novel dq transformation. Proceeding of the 38th IAS Annual Conference on Record of the Industry Applications Conference, Vol. 2, October 12-16, 2003, IEEE, Nagoya, Japan, ISBN:0-7803-7883-0, pp: 1222-1227.

Tipsuwanporn, V., A. Charoen, A. Numsomran and K. Phipek, 2011. A single-phase PWM inverter controlling base on PLL technique. Proceedings of the 2011 SICE Annual Conference on SICE, September 13-18, 2011, IEEE, Bangkok, Thailand, ISBN:978-1-4577-0714-8, pp: 1178-1183.

Wang, Z., Y. Wang and S. Wu, 2010. Enhanced single phase locked loop for grid-connected converter in distribution network. Proceeding of the 2010 International Conference on Electrical and Control Engineering (ICECE), June 25-27, 2010, IEEE, Shanghai, China, ISBN:978-1-4244-6880-5, pp: 3705-3709.