Journal of Engineering and Applied Sciences 7 (2): 152-154, 2012
ISSN: 1816-949X

Current Sensor and Compatible Test Processor for IDDQ Testing of Integrated Circuits

M.S. Amin, Md. Mamun and Mohd. Marufuzzaman
Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia, 43600 UKM, Bangi, Selangor, Malaysia

Abstract: The present state and next state of sequential circuits are not independently controllable and observable. As such, the testing of sequential circuit is complicated. This study presents an approach to design and develop a VLSI system for the simultaneous logic and IDDQ testing of CMOS ICs with mixed-mode testing facility for sequential circuits. The research involves the design of an interfacing unit on PCB containing interfacing circuits for parallel data exchange between a test processor and a microcomputer. This allows IDDQ measurement for every vector used for logic testing, performing logic testing simultaneously, providing a promising IDDQ fault coverage and reducing substantially the time and cost of testing. Three basic test development strategies are considered. They are functional test development, structural test development and physical defect test development. Mixed-mode testing facility is adopted to enhance the performance and reduce the testing time. The simulation result shows that the presence of the sensor does not degrade the normal operation of the CUT.

Key words: Current sensor, test processor, IDDQ testing, CMOS, physical defeat, Malaysia

INTRODUCTION

IDDQ testing is effective to many defects in CMOS ICs that remain undetected by logic testing (Sharma and Ravikumar, 1996). The conventional logic testing is crucial to verify functionality while IDDQ testing is an additional testing to improve reliability (Soden and Hawkins, 1989). Separate testing of logic testing and IDDQ testing increases testing time and cost. Performing both the test simultaneously is advantageous in terms of time and cost. In IDDQ testing, quiescent supply currents (IDDQ's) are measured.

Since, the quiescent supply current of a faultless CMOS IC is very small an IC can be considered faulty if a large quiescent current is measured (Thibeault and Hariri, 2011). It is shown that some defects which do not generate any effects on output logic values can be detected by the IDDQ testing. Therefore, a reliable current sensor is essential for IDDQ testing (Shen *et al*., 2010; Arumi *et al*., 2007). Three major steps are considered when developing a current sensor for a system of simultaneous logic and IDDQ testing. A current sensor that is able to handle the transient current peaks (up to 1 A), able to sense the quiescent current (in μA range) with precision (Ramirez-Angulo and Altamirano, 1996) and capable of maintaining proper power supply voltage across the CUT during testing (Tang *et al*., 1995). The sensor should be able to measure the IDDQ very fast (at 10-100 kHz test frequency). Mixed-mode pattern generation includes generation of pseudo-random vectors first and then generation of deterministic vectors. Pseudo-random test vectors generated from simple Linear Feedback Shift Register (LFSR) or other generators can cover a large percentage of easily testable faults and deterministic test vectors are then generated for random pattern resistance faults. Complete fault coverage can be achieved by this approach. Mixed-mode pattern generation needs less computation time than deterministic pattern generation and the necessary hardware circuitry is also simpler (Ul-Amin, 1998). For combinational circuits the output is a function of the present state only but for sequential circuits output depends not only on present state but on next state as well.

As the present state and next state of sequential circuits are not independently controllable and observable, therefore the testing of sequential circuit is complicated. To overcome this problem, a special design for testability methods is used in sequential circuits to force the circuit into any desired state with the incorporation of special reset logic and to observe both present and next states.

MATERIALS AND METHODS

Sensor design: This research work present the design of a current sensor and a compatible test processor for simultaneous logic and IDDQ testing of CMOS ICs. The sensor is an analog circuit and it is designed by using

Corresponding Author: M.S. Amin, Department of Electrical, Electronic and Systems Engineering,
Universiti Kebangsaan Malaysia, 43600 UKM, Bangi, Selangor, Malaysia

Design Architect EDA tool from Mentor Graphics. The performance of the sensor is evaluated by using Mentor Graphics analog simulator AccuSim. A voltage controlled switch VCS bypassed the high transient current peaks. So, it made closed before loading the IDDQ vectors to the CUT and made open when the transient current settles down. During transient, the maximum allowable shifting of voltage at the ground pin of the CUT is considered 0.2 V (Ramirez-Angulo and Altamirano, 1996). Therefore, the on resistance of VCS is set to 0.2 Q so that the sensor can handle transient current peaks up to 1 A. The OP AMP is used to maintain virtual ground at the CUT's ground pin so that ground level does not shift during IDDQ monitoring.

The test processor: The test processor is a digital circuit and is designed by using VHDL programming. It is microcomputer controlled and is designed to generate the test vectors and to apply them to CUT, to capture the output responses and to compress them and at the same time to control the sensor and to receive the IDDQ pass/fail signal from the sensor. The test processor is able to generate mixed-mode test vectors for both combinational and sequential circuits. Test vectors generated based on user programmable multiple polynomials multiple seed LFSR scheme. It is facilitated for storing 16 sets of seeds and corresponding polynomials in the memory elements of the test processor which in turn generate 16 sets of test vectors. A top down fashion with mixed-mode technique is used to design the test processor. It began with a high level abstract model that describes only the desired behavior to be realized by the circuit and then a few modules follow the structural modeling.

The initialization sequence which take the CUT from an unknown starting state to a known state is incorporated with a reset logic and then the observation sequence make the result of the state transition observable from the present state. This logic is adopted towards the design for testability methods of sequential circuits to force the circuit into any desired state to observe both present and next states.

RESULTS AND DISCUSSION

The c17 benchmark circuit is used as example CUTs for the purpose of simulation to show the performance of the sensor to detect different bridging faults. Figure 1

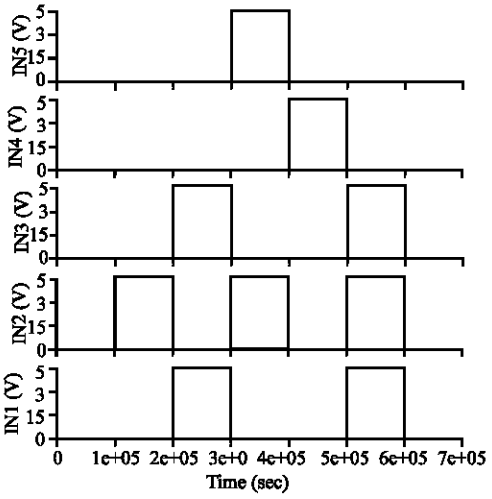

Fig. 1: About 70 μ sec input wavefprm for c17 benchmark (Analog trace)

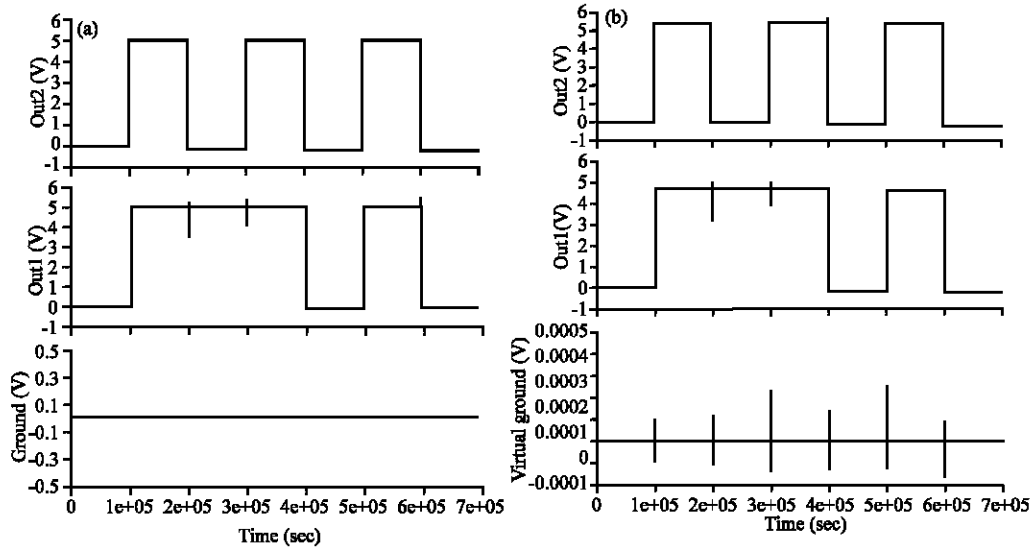

Fig. 2: Response of fault-free c17; a) without sensor; b) with senor (Analog trace)

shows an arbitrary input waveform for 70 μ sec duration. Here, the waveform changes after every 10 μ sec. The response of the fault free CUT without the current sensor for this input waveform is shown in Fig. 2a, b describes the output response with the sensor connected to the fault-free CUT. The output responses of Fig. 2a, b are similar and this implies that the presence of the sensor does not degrade the normal operation of the CUT.

CONCLUSION

Three basic test development strategies are considered. They are functional, structural and physical defect test development. Mixed-mode testing facility is adopted to enhance the performance and reduce the testing time. The simulation result shows that the presence of the sensor does not degrade the normal operation of the CUT.

REFERENCES

Arumi, D., R. Rodriguez-Montanes, J. Figueras, S. Eichenberger, C. Hora, B. Kruseman and M. Lousberg, 2007. IDDQ-based diagnosis at Very Low Voltage (VLV) for bridging defects. Electron. Lett., 43: 25-26.

Ramirez-Angulo, J. and G.G. Altamirano, 1996. High speed IDDQ current sensors for VLSI system testing. IEEE Int. Symp. Circuits Syst., 1: 389-392.

Sharma, N. and C.P. Ravikumar, 1996. Improving bridge-fault testability and confidence of IDDQ testing through circuit placement. Proceedings of the International Workshop on IDDQ Testing, October 24-25, 1996, Washington, DC, USA., pp: 20-24.

Shen, S.T., C. Liu, E.H. Ma, I.C. Cheng and J.C.M. Li, 2010. Reliability screening of a-Si TFT circuits: Very-low voltage and I_{DDQ} testing. J. Disp. Technol., 6: 592-600.

Soden, J.M. and C.F. Hawkins, 1989. Electrical properties and detection methods for CMOS IC defects. Proceedings of the 1st European Test Conference, April, 12-14, 1989, Paris, France, pp: 159-167.

Tang, J.J., K.J. Lee and B.D. Liu, 1995. A Practical current sensing technique for IDDQ testing. IEEE Trans. Sys., 3: 302-310.

Thibeault, C. and Y. Hariri, 2011. Improving current-based testing and diagnosis through modified test pattern generation. IEEE Trans. Very Large Scale Int. Sys., 19: 130-141.

Ul-Amin, M.A., 1998. An approach to current sensor and test processor design for simultaneous logic and iddq testing of cmos integrated circuits. Masters Thesis, Faculty of Engineering, Universiti Kebangsaan Malaysia, Malaysia.