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Analysis and Application of Hybrid MOSFET Structure for Low Gate Leakage

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Abstract: A novel Hybrid MOSFET (HMOS) structure has been proposed to diminish the gate leakage current significantly. This novel Hybrid MOSFET (HMOS) consist of source/drain-to-gate non-overlap region and high-k layer/interfacial oxide as gate stack. Vertical fringing electric field through the high-k dielectric spacer induces inversion in the non-overlap region to act as extended S/D. The gate leakage behaviour of HMOS has been investigated with the help of compact analytical model and Sentaurus simulation. The model sustains a very good agreement between the model and TCAD result. It is found that HMOS structure has reduced the gate leakage current to great extent as compared to conventional overlapped MOSFET structure. Further, the proposed structure had demonstrated improved on current, off current, subthreshold slope and DIBL characteristic.

Key words: Hybrid MOSFET (HMOS), gate tunneling current, analytical model, spacer dielectrics, DIBL, subthreshold slope

INTRODUCTION

The successful scaling of MOSFETs toward shorter channel lengths requires thinner gate oxides and higher doping levels in order to achieve high drive currents and minimized short channel effects (Ono *et al*., 1995; Taur *et al*., 1997). In this situation, the gate leakage current due to tunnelling through gate oxide becomes very high. Gate leakage is predicted to increase at a rate of <500x per technology generation while sub-threshold leakage increases by around 5x for each technology generation. Thus to reduce the gate leakage current in present era of integrated circuits, new device structures are needed as a method to contain/reduce the gate leakage current especially for low power battery operated portable applications (Taur, 2002).

In the past, various techniques have been proposed to control the gate leakage currents. The researchers (Sirisantana *et al*., 2000) presents an approach to reduce I_{sub} but not I_{gate}. The impact of I_{gate} on delay is discussed (Choi *et al*., 2001) but its impact on leakage power is not addressed. Hamzaoglu and Stan (2002) presented circuit level techniques for gate leakage minimization. In each of these reports, extensive SPICE simulations were performed to obtain estimates of gate leakage. Roy *et al*. (2003) addressed various leakage mechanisms including gate leakage and presented circuit level technique to reduce the leakage. However, this can be extremely time consuming, especially for large circuits. Lee *et al*. (2003) examine the interaction between I_{gate} and I_{sub} and their state dependencies. This research applies pin reordering to minimize I_{gate}. Lee *et al*. (2004) developed a method for analyzing gate oxide leakage current in logic gates and suggested pin reordering to reduce it. Sultania *et al*. (2004) developed an algorithm to optimize the total leakage power by assigning dual T_{ox} values to transistors. Sirisantana and Roy (2004) use multiple channel lengths and multiple gate oxide thickness for reduction of leakage. Mohanty and Kougianos (2006) have presented analytical models and a data path scheduling algorithm for reduction of gate leakage current.

Conventional offset gated MOSFET structure has been widely used to reduce subthreshold leakage but gate leakage reduction has not been addressed in the literature so far (Lee *et al*., 2002). Thus, the general problems of gate leakage reduction techniques are the need for additional devices (e.g., sleep transistors) and the reduction of only one component of leakage. Moreover, transistor level approaches are not applicable for standard cell designs and require long calculation time. Further, gate level DVT-/DTOCMOS methods do not offer the best possible solution as the number of gate types limits the improvement. To solve this problem, we propose Hybrid MOSFET (HMOS) structure for the first time to reduce the gate leakage current significantly because gate leakage current through the source/drain overlap region has been

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identified as the principal source of power dissipation in VLSI chips especially in sub-1V range (Ghani *et al*., 2000). The use of high-k as gate dielectric, further reduces the gate leakage current by increasing the physical thickness of the gate dielectric through which carrier tunnel. Also by adopting high-k dielectric spacers, we can induce low resistance inversion layer as a S/D extension region in the non-overlap region. An effective and compact model has been developed for analyzing the gate tunneling current of HMOS by considering the NSE (nano scale effect) effect that are difficult to ignore at nano scale regime. The NSE effect include:

- The non-uniform dopant profile in poly-gate in vertical direction resulted due to low energy ion implantation
- Additional depletion layer at the gate edges due to gate length scaling down
- Gate oxide barrier lowering due to image charges across the Si/SiO_2 interface. We also adopted advanced physical models in the simulation (Sentaurus simulator) to see other device characteristics such as DIBL (Drain Induced Barrier Lowering), SS (Subthreshold Slope) on current and off current

MATERIALS AND METHODS

In this study, we have considered inelastic trap assisted tunneling as a two step process for simplicity. Firstly, electrons tunnel into deep lying trap state, become released from the trap state and subsequently tunnel to gate under the influence of the applied electric field. Because of non overlap region between gate-to-source and gate-to-drain, the edge direct tunneling current is absent and hence, total gate leakage current (I_g) is given by:

$$I_g = I_{gc} = J_{ITAT\_ch} \times L_g \quad (1)$$

where, I_{gc} is the gate tunneling current through channel region and J_{ITAT_ch} is the inelastic trap-assisted tunneling current density through channel region and is given by a detailed balance of J_{in} and J_{out}. The J_{in} and J_{out} are tunneling-in current density from inversion layer to the traps and tunneling-out current density from the traps to the gate, respectively.

Now, assuming that x is the distance from the $Si\text{-}SiO_2$ interface, $N_{trap}(x, E)$ is the sheet trap density in cm^2 at a distance x and having the energy level with respect to the conduction band edge of gate dielectric, $O_t(x, E)$ is the electron occupancy of the traps at a distance of x and the energy of E, σ_t is the capture cross section of the traps and A_g is the gate tunneling area:

$$J_{in} = \frac{q}{A_g}\sigma_t N_{trap}\left(x, qE_{gi}x - \phi_{b\_eff}\right)\times \left[1 - O_t\left(x, qE_{gi1}x - \phi_{b\_eff}\right)\right]J_1\left(\phi_{b\_eff}, x, E_{gi1}\right) \quad (2)$$

$$J_{out} = \frac{q}{A_g}\sigma_t N_{trap}\left(x, qE_{gi1}x - \phi_{b\_eff}\right)\times O_t\left(x, qE_{gi1}x - \phi_{b\_eff}\right)J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right) \quad (3)$$

$$\phi_t = \phi_{b\_eff} - qE_{gi1}x + E_{LOSS}$$

Where:

ϕ_t = Barrier height of the gate insulator trap states
E_{gi} = Electric field in the gate insulator
E_{gi1} = Electric field over a distance x of the trap relative to the interface in the gate insulator
E_{gi2} = Electric field over a distance t_{gi} - x relative to the interface in the gate insulator
E_{loss} = Energy loss accompanied with the injection of electrons into the neutral trap sites and σ_t is assumed to be constant irrespective of the position and energy level of the traps
J_1, J_2 = Uniform current densities and are calculated by modifying the formulation of direct tunneling in Lee and Hu model (Lee and Hu, 2001)
ϕ_b = Interface barrier height of composite gate dielectric, i.e., combination of interfacial oxide and high-k gate dielectric

It is taken as the average of barrier height of interfacial oxide and high-k gate layer. So:

$$\phi_b = \frac{(\phi_{b\_ox} + \phi_{b\_hk})}{2} \quad (4)$$

Where:

ϕ_{b_hk} = Barrier height of high-k gate layer
ϕ_{b_ox} = Barrier height of oxide layer
ϕ_{b_eff} = Effective barrier height

$$\phi_{b\_eff} = \phi_b - \Delta\phi \quad (5)$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\varepsilon_{eff}}} = \sqrt{\frac{qV_{gi}}{4\pi\varepsilon_{eff}T_{gi}}} = \left(\frac{2q^3 N_{DTC(ch)}\phi_{b\_eff}}{16\pi^2\varepsilon_{eff}^3}\right)^{1/4} \quad (6)$$

The $\Delta\phi$ is the reduction in the barrier height at the high-k/SiO_2/Si interface from ϕ_b so that barrier height becomes ϕ_{b_eff}. This reduction in barrier height is due to image charges across the interface. This barrier reduction

is of great interest since it modulates the gate tunneling current. $N_{DTC(ch)}$ is the effective density of carrier in channel and ε_{eff} is the equivalent dielectric constant of composite gate dielectric. We have found the equivalent dielectric constant of the composite gate dielectric in terms of the oxide thickness by considering the MOSFET as parallel plate capacitor with two dissimilar dielectrics:

$$\varepsilon_{eff} = \left[\frac{t_{ox}}{\varepsilon_{ox} t_{gi}} + \frac{t_{gi} - t_{ox}}{\varepsilon_{hk} t_{gi}}\right]^{-1} \quad (7)$$

Where:

ε_{eff}, ε_{ox}, ε_{hk} = The dielectric constants of the equivalent dielectric, interfacial oxide and the high-k gate dielectric, respectively

t_{gi} = The total thickness of the gate dielectric

t_{ox} = The thickness of interfacial oxide Consequently, inelastic trap assisted tunneling current can be expressed as:

$$J_{ITAT} = \frac{q}{A_g}\sigma_t N_{trap}\left(x, qE_{gi}x - \phi_{b\_eff}\right)P_{ITAT}\left(x, E, E_{gi}\right) \quad (8)$$

where, P_{ITAT} can be expressed as:

$$P_{ITAT} = \frac{J_1\left(\phi_{b\_eff}, x, E_{gi1}\right)J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right)}{J_1\left(\phi_{b\_eff}, x, E_{gi1}\right) + J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right)} \quad (9)$$

Using Gauss's law and considering MOS capacitor equivalent circuit, the local electrical fields E_{gi1} and E_{gi2} of both the tunneling regions finally become:

$$E_{gi1} = E_{gi} + \frac{t_{gi} - x}{t_{gi}}.\frac{qN_{trap}}{\varepsilon_{eff}} \quad (10)$$

$$E_{gi2} = E_{gi} + \frac{x}{t_{gi}}.\frac{qN_{trap}}{\varepsilon_{eff}} \quad (11)$$

The modified uniform current density J_1 and J_2 are expressed as:

$$J_1\left(\phi_{b\_eff}, x, E_{gi1}\right) = A_t\frac{C_{(ch)}\left(\phi_{b\_eff}, x, E_{gi1}\right)}{\phi_{b\_eff}}\times \exp\left[-\frac{8\pi\sqrt{2m_{eff}}}{3hq}.\frac{\phi_{b\_eff}^{\frac{3}{2}}}{E_{gi1}}\beta\left(\phi_{b\_eff}, x, E_{gi1}\right)\right] \quad (12)$$

$$J_2\left(\phi_{b\_eff}, x, E_{gi1}\right) = A_t\frac{C_{(ch)}\left(\phi_t, t_{gi} - x, E_{gi2}\right)}{\phi_t}\times \exp\left[-\frac{8\pi\sqrt{2m_{eff}}}{3hq}.\frac{\phi_t^{\frac{3}{2}}}{E_{gi2}}\beta\left(\phi_t, t_{gi} - x, E_{gi2}\right)\right] \quad (13)$$

Where:

$$A_t = \frac{q^3}{8\pi\phi_{b\_eff}\varepsilon_{eff}}$$

$$c_{(ch)}\left(\phi_{b\_eff}, x, E_{gi1}\right) = \exp\left[\frac{20}{\phi_{b\_eff}}\left(\frac{x\left|E_{gi1(ch)}\right| - \phi_{b\_eff}}{\phi_{b\_eff}} + 1\right)^{\alpha(ch)}\left(1 - \frac{x\left|E_{gi1(ch,ov)}\right|}{\phi_{b\_eff}}\right)\right]\times \left(E_{gi1}\right)N_{DTC(ch)}$$

$$c_{(ch)}\left(\phi_t, t_{gi} - x, E_{gi2}\right) = \exp\left[\frac{20}{\phi_t}\left(\frac{(t_{gi} - x)\left|E_{gi2(ch)}\right| - \phi_t}{\phi_t} + 1\right)^{\alpha(ch)}\left(1 - \frac{(t_{gi} - x)\left|E_{gi2(ch,ov)}\right|}{\phi_t}\right)\right]\times \left(E_{gi2}\right)N_{DTC(ch)}$$

$$\beta(\phi_{b\_eff}, x, E_{gi1}) = 1 - \left(1 - \frac{qx}{\phi_{b\_eff}}\left|E_{gi1}\right|\right)^{3/2}$$

$$\beta(\phi_t, t_{gi} - x, E_{gi2}) = 1 - \left(1 - \frac{q\left(t_{gi} - x\right)}{\phi_t}\left|E_{gi2}\right|\right)^{3/2}$$

$$N_{DTC(ch)} = \begin{cases} \frac{\varepsilon_{eff}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1 + \exp\left(-\frac{\left(V_g - V_{FB}\right)}{n_{acc}v_t}\right)\right]\right. & \text{for } V_g < 0 \\ \frac{\varepsilon_{eff}}{t_{gi}}\left\{n_{inv}v_t.\ln\left[1 + \exp\left(-\frac{\left(V_g - V_{th}\right)}{n_{inv}v_t}\right)\right]\right. & \text{for } V_g > 0 \end{cases}$$

where, m_{eff} is the equivalent effective mass of the composite dielectric. Taking the resistances in series of the two layers of the gate dielectric we have:

$$R_{gi} = R_{ox} + R_{hk} \quad (14)$$

Considering the relaxation time $\tau_{ox} = \tau_{hk} = \tau_{eff} = \tau$, we obtain the equivalent effective mass of composite gate dielectric using Eq. 14 as:

$$m_{eff} = \left[\frac{m_{ox} t_{ox}}{t_{gi}} + \frac{m_{hk}\left(t_{gi} - t_{ox}\right)}{t_{gi}} \right] \quad (15)$$

Where:

$\alpha_{(ch)}$ = Fitting parameter for channel region tunneling
n_{inv}, n_{acc} = Swing parameters
V_{FB} = Represents the flat band voltage
$N_{DTC(ch)}$ = Denotes the density of carrier in channel region depending upon MOSFET biasing condition
$C_{F(ch, ov)}$ = Correction factor
V_{ge} = Effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to V_g- V_{poly}

The default values of n_{inv} and n_{acc} are S/v_t (S is the sub threshold swing and v_t is the thermal voltage) and 1, respectively. M_{ox} is the effective mass of electrons in the interfacial oxide layer and m_{hk} is the same in the high-k gate dielectric layer. The voltage across the gate insulator for different region of operation is as follows:

$$V_{gi} = \begin{cases} \left(V_g - \phi_s - V_{FB}\right) \text{ for } V_g < 0 \\ \left(V_{ge} - \phi_s - V_{FB}\right) \text{ for } V_g > 0 \end{cases} \quad (16)$$

Where, ϕ is the surface band bending of the substrate for channel depending upon the biasing condition of the MOSFET device including the poly non-uniformity, gate length effects and image force barrier lowering. The accurate surface potentials expressions in case of channel in weak inversion/depletion, strong inversion and in accumulation can be taken from (Pregaldiny *et al*., 2004). The effective gate voltage including the effect of nonuniform dopant distribution in the gate is derived as follows:

$$V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) + \frac{\left(q\varepsilon_{si} N_{poly} T_{gi}^2\right)}{\varepsilon_{ox}^2} \left[\sqrt{1 + \frac{2\varepsilon_{gi}^2 (V_g - V_{FB} - \phi_{so})}{q\varepsilon_{si} N_{poly} T_{gi}^2}} - 1 \right] \quad (17)$$

The ϕ_{so} by taking the quantization effect into account is given (Taur and Ning, 1998) as follows:

$$\phi_{so} = 2\phi_s + \Delta\phi_s^{QM} - V_{BS} \quad (18)$$

Where, ϕ_s^{QM} can be taken from Pregaldiny *et al*. (2004). This equation (Lee and Hu, 2001) includes the non uniformity in the gate dopant profile through a term ΔV_{p1} and fringing field effect, i.e., gate length effect through a term Δv_{p2}. The potential drop ΔV_{p1} due to non uniform dopant profile in poly Si gate, caused by low energy implantation is given by:

$$\Delta V_{p1} = \left(\frac{kT}{q}\right) \ln\left(\frac{N_{poly\_top}}{N_{poly\_bottom}}\right) \quad (19)$$

The N_{poly_top} and N_{poly_bottom} are the doping concentration at the top and bottom of the polysilicon gate. The potential drop ΔV_{p2} due to gate length effect caused by very short gate lengths is given as:

$$\Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qAN_d}{L_g C_d} \left(V/cm\right) \quad (20)$$

$$C_d = \delta \frac{\varepsilon_{eff}}{\pi} \ln\left[\frac{3 - \cos\left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}}{1 + \left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}} \right] \quad (21)$$

Where:

A = Denote the triangular area of the additional charge
L_g = Gate length
C_d = Depletion capacitance in the sidewalls (Chung and Li, 1992)
ε_{eff} = Effective permittivity of the composite gate insulator
T_F = Thickness of the field oxide
T_{gi} = Thickness of the gate insulator
δ = Fitting parameter equal to 0.95 normally

Device design: The cross-section of HMOS for the analysis of the gate tunneling current characteristics is shown in Fig. 1. The MOSFET has n^+ poly-Si gate of

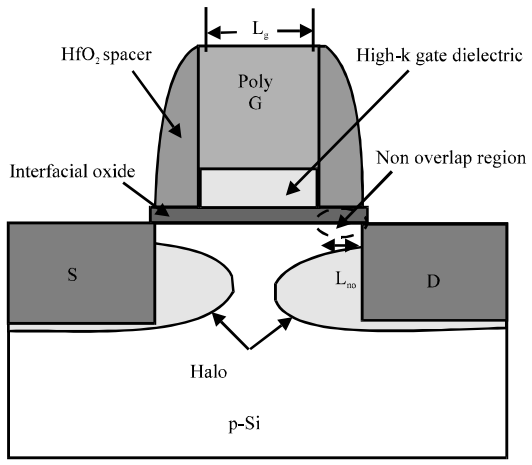

Fig. 1: Schematic cross-section of proposed Hybrid N-MOSFET

physical gate Length (L_g) of 35 nm, gate dielectric of 1.0 nm EOT (Equivalent Oxide Thickness) -0.3 nm interfacial oxide and 0.7 nm EOT of high-k gate dielectric. The buffer oxide of 1.0 nm under high-k spacer has been taken to minimize the stress between spacer and substrate. Here, L_{no} represents the non-overlap length between gate to source/drain.

The source/drain extension region are created with the help of fringing gate electric field by inducing an inversion layer in the non overlap region. So, HfO_2 high-k dielectric is used as spacer because, it develops high vertical electric field under non-overlap region to induce inversion layer.

The halo doping around the S/D also reduces short-channel effects such as the punch-through current, DIBL and threshold voltage roll-off for different non-overlap lengths.

Simulation set up: Figure 2 shows the santaurus simulator schematic of HMOS. The doping of the silicon S/D region is assumed to be very high, 1×10^{20} cm^{-3} which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 40 nm long and 20 nm high. This gives a large contact area resulting in a small contact resistance.

The doping concentration in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of 1×10^{18} and 1×10^{17} cm^{-3} near the channel. The poly silicon doping has been taken to be 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at bottom of the polysilicon gate, i.e., interface of oxide and silicon.

The MOSFET was designed to have Vth of 0.25 V. We determined Vth by using a linear extrapolation of the linear portion of the I_{DS}-V_{GS} curve at low drain voltages. The operating voltage for the devices is 1.0 V. The simulation

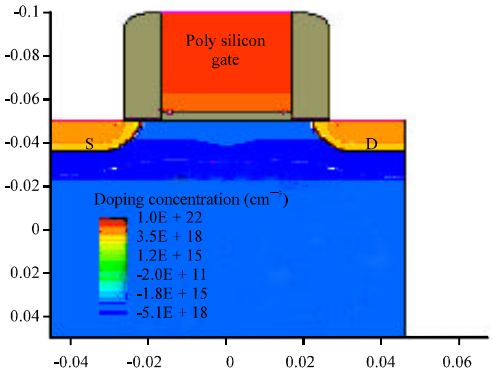

Fig. 2: Sentaurus schematic cross-section of HMOS

study has been conducted in 2 dimensions hence, all the results are in the units of per unit channel width. The simulation of the device is performed by using Santaurus design suite (Taur and Ning, 1998) with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

Figure 3 shows the simulated vertical electric field along the channel direction for different spacer in the non-overlap region for non-overlap length of 5 nm. The vertical electric field is plotted for 3 different spacer such as HfO_2 (k = 22), Si_3N_4 (k = 7.5) and SiO_2 (k = 3.9). It is clear (Fig. 3) that magnitude of vertical electric field increases with the increase in dielectric constant of the spacer.

The vertical electric filed is responsible to induce an inversion layer in the non-overlap region. Result shows that approximately 3 times higher vertical electric field is obtained under non-overlap region by HfO_2 high-k spacer compared to the oxide spacer.

This implies that the on-state current of the high-k spacer non-overlapped gate to S/D MOSFET can be significantly larger than that of the oxide spacer MOSFET.

This guides the use of compatible high-k spacer (i.e., compatible HfO_2) to induce the sufficient inversion layer in non-overlap region. It also shows that vertical electric field magnitude decreases significantly with the distance of non overlap region from the gate edge there by limiting the non-overlap length (L_{no}).

Figure 4 plots the variation of vertical electric along the channel direction with HfO_2 spacer in the non overlap region for different gate dielectrics, i.e., SiO_2, Si_3N_4 and

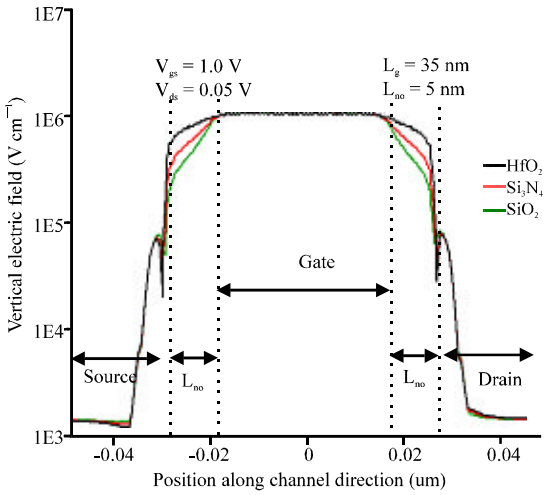

Fig. 3: Vertical electric field along channel for different spacer in the non overlap region

HfO_2. It is clear from Fig. 4 that the magnitude of vertical electric field is almost constant with change of gate dielectric. The fringing electric field is a strong function of dielectric constant of spacer material instead of dielectric constant of gate dielectric material. It Is observed from Fig. 5 that electron concentration below the spacer also remains constant with the change of dielectric constant of gate dielectric.

This is due to that fact that vertical fringing field remains constant with the change of dielectric constant of dielectric. However, it is obvious that the vertical fringing electric field produced by HfO_2 high-k spacer is capable of inducing electron concentration of the order of 1×10^{-18} cm^{-3} which in turn can behave as extended S/D region. Thus, a reasonable amount of electron concentration was induced for HfO_2 spacer.

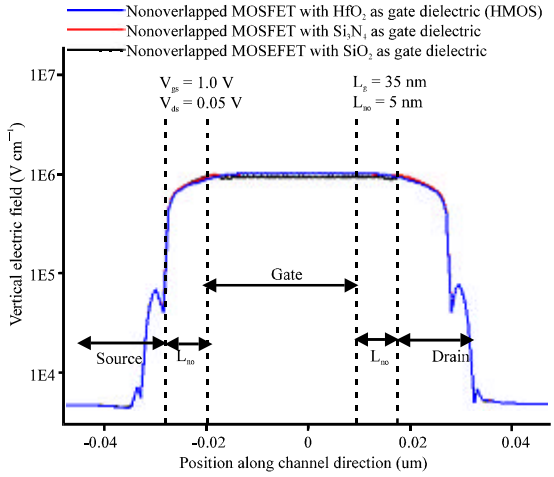

Fig. 4: Vertical electric field along channel with HfO_2 spacer in the non overlap region for different gate dielectrics, i.e., SiO_2, Si_3N_4 and HfO_2

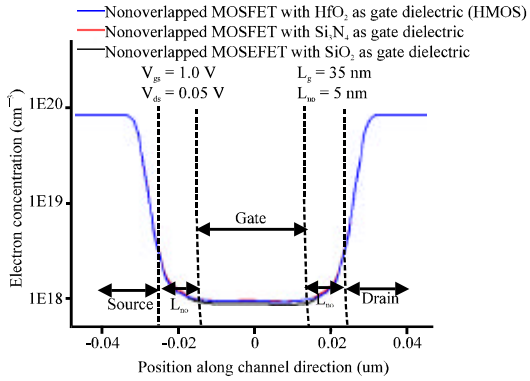

Fig. 5: Electron concentration along channel with HfO_2 spacer in the non overlap region for different gate dielectrics, i.e., SiO_2, Si_3N_4 and HfO_2

RESULTS AND DISCUSSION

Computation have been carried out for a n-channel nanoscale Hybrid MOSFET (HMOS) to estimate the gate tunneling current. The interfacial oxide thickness and EOT for high-k gate dielectric have been taken to be 0.3 and 0.7 nm, respectively with a combined EOT of 1.0 nm. This model is computationally efficient and easy to realize. The comparision between the simulated data and the model data for gate tunneling current is shown in Fig. 6. The Fig. 6 shows the gate tunneling current versus gate bias for HMOS with HfO_2 spacer above the non-overlap region at an Equivalent Oxide Thickness (EOT) of 1 nm and non-overlap length of 5 nm.

It is shown in Fig. 6 that analytical result calculated by the model has better agreement with the simulated results certifying the high accuracy of the propsed analytical modelling.

The simulation for HMOS with HfO_2 as high-k gate dielectric has been carried out with t_{HfO_2} = 3.95 nm, $t_{interfacial\_oxide}$ = 0.3 nm. ϕ_{b_hk} (HfO_2) =1.5 ev, m_{hk} = 0.18 m_o (Tyagi and George, 2008), σ_t = 9.3×10^{-16} cm^2 (Chen *et al*., 2008), N_{trap} = 7.67×10^{12} cm^{-2} (Chen *et al*., 2008). The trap position (x_t) is extracted to be 0.35 t_{HfO_2} in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 3.95 nm. The fitting parameters E_{loss} and $\alpha_{(ch)}$ have been taken to 0.36 eV, 0.62, respectively to fit the model with the simulated value. Figure 7 shows the variation of the gate tunneling current with gate bias for different gate dielectrics of HMOS. It is observed that gate leakage current decreases significantly for HMOS compared to overlapped conventional

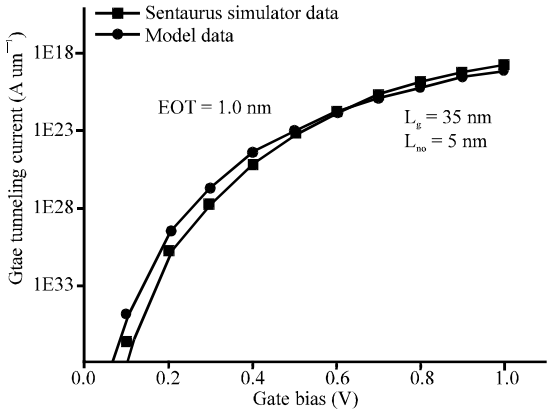

Fig. 6: Comparison of analytical model data with Sentaurus simulated data HMOS with Equivalent Oxide Thickness (EOT) of 1.0 nm, physical gate length of L^g = 35nm and S/D to gate non overlap length of L^{no} = 5 nm

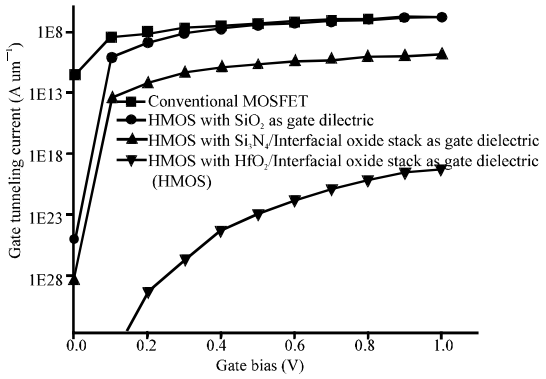

Fig. 7: Gate tunneling current vs. gate bias for HMOS with different gate dielectrics, e.g., SiO_2, Si_3N_4 and HfO_2

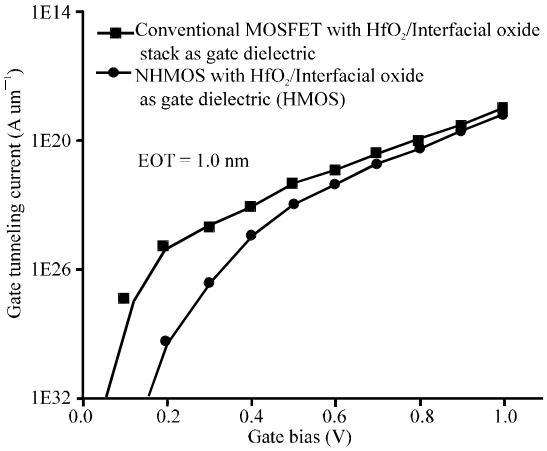

Fig. 8: Gate tunneling current vs gate bias for HfO_2 based high-k HMOS and overlapped HfO_2 based high-k conventional MOSFET at an EOT of 1.0 nm

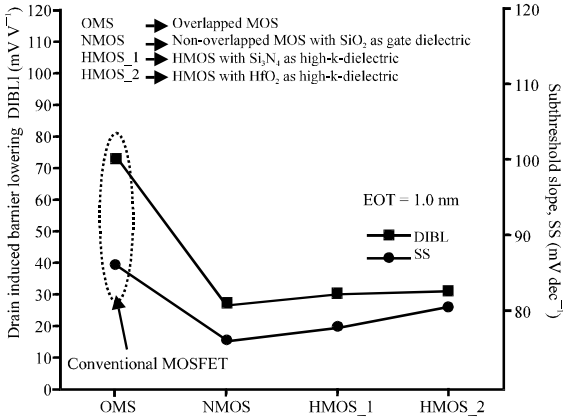

Fig . 9: DIBL, SS for HMOS with different gate dielectrics, e.g., SiO_2, Si_3N_4 and HfO_2 at an EOT of 1.0 nm

structure. This is because gate to S/D overlap region is absent in the designed HMOS so, gate tunneling (leakage) current is reduced to greater extent. The reduction is significant with the increase of dielectric constant of gate dielectric of HMOS. This is because vertical electric field responsible for carrier tunneling decreases as the physical thickness of gate insulator increases with increase in dielectric constant (k). The simulation for HMOS with Si_3N_4 high-k gate dielectric has been carried out with t_{Si3N4} = 1.35 nm, $t_{interfacial\_oxide}$ = 0.3 nm. ϕ_{b_hk} (Si_3N_4) =2.0 ev, m_{hk} = 0.20 m_o (Tyagi and George, 2008), $\sigma_t = 3\times10^{-13}$ cm^2 (Vishnyakov *et al.*, 2009), $N_{trap} = 3\times10^{-11}$cm^2 (Sekine *et al.*, 2000).

The trap position (x_t) is extracted to be 0.29 t_{Si3N4} in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 1.35 nm. The fitting parameters E_{loss} and $\alpha_{(ch)}$ has been taken to 0.23 eV and 0.71, respectively to fit the model with the simulated value.

Figure 8 plots the gate tunneling current with gate bias for HfO_2 based high-k HMOS and overlapped HfO_2 based high-k conventional MOSFET at an EOT of 1.0 nm. It is observed that gate leakage current decreases significantly for HfO_2 based high-k HMOS as compared to overlapped HfO_2 based high-k conventional MOSFET especially at low gate bias range.

At low gate bias, channel is about to form so that gate leakage current is mainly due to carrier tunneling through gate to S/D overlap region. The gate to S/D overlap region is absent in the designed HfO_2 based high-k HMOS so gate tunneling (leakage) current is reduced to greater extent. However, at higher gate bias range the gate tunneling (leakage) current is mainly due to the carrier tunneling through the channel region to the gate. Due to this reason, gate tunneling current is almost same for both structure. Figure 9 shows the variation of DIBL and SS for HMOS with different gate dielectrics, e.g., SiO_2, Si_3N_4 and HfO_2 at an EOT of 1.0 nm. It is shown in Fig. 9 that DIBL is maximum (72.55 mV/V) for overlapped gate to S/D MOSFET structure (conventional MOSFET). It is due to the fact that the effect of fringing field on channel is maximum.

Due to this decrease in gate control, the drain electrode is tightly coupled to the channel and the lateral electric field from the drain reaches a larger distance into the channel. Consequently, this electrically closer proximity of drain to source gives rise to higher Drain-Induced Barrier Lowering (DIBL) in overlapped gate to S/D MOSFET structure. In non-overlapped gate to S/D

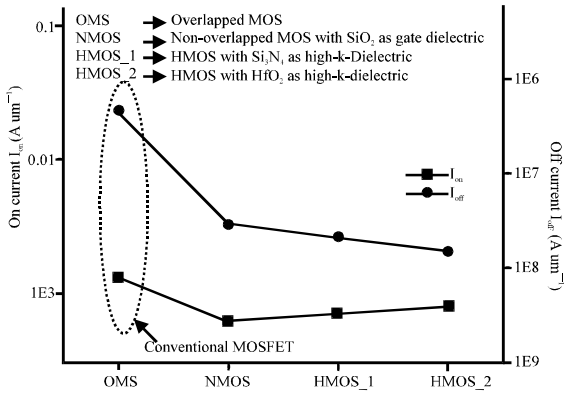

Fig . 10: On and off current HMOS with different gate dielectrics e.g. SiO_2, Si_3N_4 and HfO_2 at an EOT of 1.0 nm

MOSFET Structure (NMOS), DIBL improves because lateral electric field from the drain reaches a smaller, distance into the channel.

This is due to increase in metallurgical gate length as compared to conventional MOSFET structure in the same physical gate length. For HMOS with Si_3N_4 (HMOS_1) and HfO_2 (HMOS_2) gate dielectric, DIBL degrades due to increased coupling of lateral electric field from the drain into the channel because of slightly enhanced fringing field. It is also shown in Fig. 9 that subthreshold characteristic improves for non overlapped gate to S/D MOSFET structure(NMOS) compared to overlapped gate to S/D conventional MOSFET structure. But for HMOS with Si_3N_4 (HMOS_1) and HfO_2 (HMOS_2) gate dielectric, SS degrades due to increased the depletion capacitance in the subthreshold equation. Figure 10 shows the on and off current behavior of HMOS with different gate dielectrics, e.g., SiO_2, Si_3N_4 and HfO_2. It is showed in Fig. 10 that on current slightly degrades and off current slightly improves with increase in dielectric constant of gate dielectric due to increase in threshold voltage (Vth). The I_{on}/I_{off} ratio $>3\times10^4$ is achievable for NMOS follow by HMOS_1, HMOS_2 and conventional MOSFET. The result indicates that non overlapped gate to S/D NMOSFET (NMOS) is better in term of SCE whereas HMOS_2 is better in term of gate leakage reduction.

CONCLUSION

This study examines the gate leakage current of 35 nm HMOS by using simplified and compact analytical gate current model including Nano Scale Effect (NSE). It is demonstrated that the HMOS exhibits a significantly diminished gate leakage current leading to several orders of magnitude reduction in the OFF state leakage current when compared to a conventional MOSFET. The model proposed here is very simple in practical applications. Furthermore, it sustains a very good agreement between the model and TCAD result. This is very useful in circuit design that the gate leakage current could be taken into consideration in performing the circuit simulations.

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