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A New ZVCS CLL Resonant Push-Pull DC-DC Converter Topology

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Abstract: A new ZVCS CLL resonant push-pull DC-DC converter is presented in which the resonant circuit is located at the secondary side of the transformer. The proposed converter topology is suitable for unregulated low voltage to high voltage power conversion, as in battery- powered system. The MOSFET primary switches and output rectifier turn-on and turn-off operate under zero-voltage and zero-current switching conditions. Circuit simulations and experimental results are presented and are shown to have excellent agreement with fundamental mode analysis.

Key words: ZVCS, resonant converter, push-pull converter, step-up converter

INTRODUCTION

The Series (SRC) and Parallel Resonant Converters (PRC) are examples of topologies with two reactive energy storage elements. These circuits are widely used but have limitations that preclude their employment in many applications.

There are several reasons for studying three element topologies one is removing these limitations. Another is that parasitic L and C is often present. This can force a nominally two-element topology to actually operate as three or four elements. It is necessary to understand the behavior of these higher order topologies. A less obvious reason is the insight gained from studying a new family of converters topologies even when they may not have immediate applications. Every time we add on other piece to the power converter puzzle we learn something about the whole.

In three element resonant tank there are 36 different configurations (Severns, 1992; Batarzed, 1994; Anonymes, 1989; Liu and Lee, 1992). For voltage source input application only 23 resonant tank are suitable. Within these 23 resonant tank configurations, three resonant tanks show desired characteristics (Lazar and Martinelli, 2001; Elferich and Duerbaum, 2002; Yang *et al*., 2002a,b). The three resonant tanks are shown in Fig. 1.

The LCL-Resonant push-pull DC-DC converter topology (Liu and Lee, 1986; Shoyama and Harada, 1991; Ryan *et al*., 1995) is implemented using Resonant Tank U. It operates under zero-voltage switching condition where the input current can exceed input voltage by an order of magnitude with high efficiency.

Since the output load of the LCL topology is series connected with the output resonant inductor, so the output current will swing corresponding to the resonant current and it is difficult to decrease or control the ripple output voltage. So Boonyaroonate and Mori (2002) demonstrate resonant push-pull DC-DC converter with low ripple output voltage. He proposed series resonant circuit in the converter.

The impedance of the parallel resonant circuit is high compared to series resonant circuit. So loading on the

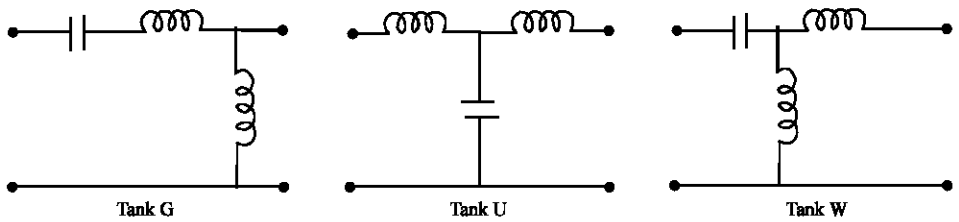

Fig. 1: Resonant tanks

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input side is very much reduced by using parallel resonant circuit. In this paper, we proposed the ZVCS CLL quasi-resonant push-pull DC-DC converter with resonant tank W.

CIRCUIT DESCRIPTION

The proposed DC-DC converter is based on push-pull DC-DC converter and it consists of MOSFET primary switches (S_1,S_2), CLL resonant tank circuit, output rectifier (D_1-D_4), output capacitor and output load(R_L). The resonant circuit (CLL) resonates at the switching frequency of S_1 and S_2.

FUNDAMENTAL MODES OF OPERATION

The proposed DC-DC converter is shown in Fig. 2. The primary switches (S_1, S_2) are driven by the fixed frequency pulses at duty ratio below 50%, out of phase. The circuit operation modes are shown in Fig. 3a. The equivalent circuit model for each mode are shown in Fig. 3b, in which $V_s = NV_1$, where N is the transformer turn ratio. The idealized waveforms are shown in Fig. 4. The quality factor of the resonant circuit (CLL) has to below enough to keep the resonant current (i_L) discontinuous.

For each of the four modes in Fig. 3, closed form equations for circuit operation are found: damping has been ignored. These equations are listed below. Initial inductor current, inductor voltage and capacitor current at the start of each mode (when the input MOSFET's and/or output rectifier's switch) are designed as I_{L10}, V_{L20} and I_{C10} respectively. These initial conditions are found from the end values of the previous mode. Note that the terms V_0 and I_0 are redefined for each mode.

The switches M_1 and M_2 are turn-on at zero voltage and turn-off at zero current due by the resonant circuit (CLL) at the secondary side. During switch commutation the magnetizing current of the transformer will flow through the body diodes of the MOSFET's leading to zero-voltage turn on.

Mode1

$$i_{C1}(t) = I_0 + (I_{C10} - I_0)\mathrm{Cos}(\omega_0 t) + \left(\frac{(-V_s - V_{L20})}{Z_4} - \frac{(V_s + V_d)}{Z_2}\right) \mathrm{Sin}(\omega_0 t) - \frac{(V_s + V_d)}{z_2}(\omega_0 t)$$

$$I_0 = \left(\frac{(I_{C10} - L' I_{L10})}{L_2 + L'}\right)$$

$$i_{L1}(t) = I_0 + (I_{L10} + I_0)\mathrm{Cos}(\omega_0 t) + \left(\frac{(V_{L20} - V_d)}{Z_1} + \frac{(V_s + V_d)}{Z_2}\right) \mathrm{Sin}(\omega_0 t) - \frac{(V_s + V_d)}{z_2}(\omega_0 t)$$

$$V_{L2}(t) = V_0 + (V_{L20} - V_0)\mathrm{Cos}(\omega_0 t) + (I_{C10} - I_{L10})Z_3 \mathrm{Sin}(\omega_0 t)$$

$$V_0 = \left(\frac{L_2 V_d - L' V_s)}{L_2 + L'}\right)$$

Mode 2

$$i_{C1}(t) = I_0 + (I_{C10} - I_0)\mathrm{Cos}(\omega_0 t) + \left(\frac{(V_{L20} - V_s)}{Z_4} - \frac{(V_d - V_s)}{Z_2}\right) \mathrm{Sin}(\omega_0 t) + \frac{(V_d - Vs)}{z_2}(\omega_0 t)$$

$$I_0 = \left(\frac{(I_{C10} L_2 + L' I_{L10})}{L_2 + L'}\right)$$

$$i_{L1}(t) = -I_0 + (I_{L10} - I_0)\mathrm{Cos}(\omega_0 t) + \left(\frac{(V_{L20} - V_d)}{Z_1} + \frac{(V_s - V_d)}{Z_2}\right) \mathrm{Sin}(\omega_0 t) + \frac{(V_s - V_d)}{z_2}(\omega_0 t)$$

$$V_{L2}(t) = V_0 + (V_{L20} - V_0)\mathrm{Cos}(\omega_0 t) + (-I_{C10} - I_{L10})Z_3 \mathrm{Sin}(\omega_0 t)$$

$$V_0 = \left(\frac{L_2 V_d - L' V_s)}{L_2 + L'}\right)$$

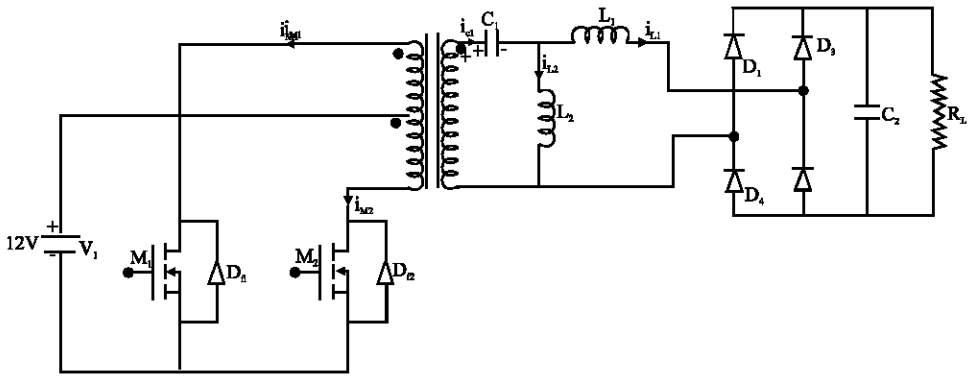

Fig. 2: CLL Resonant push-pull DC-DC converter topology

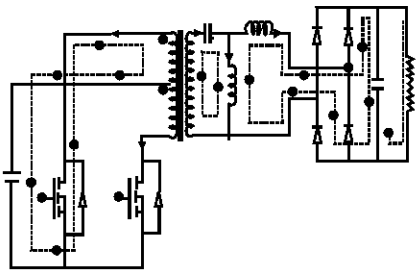

Fig. 3. (a) Mode 1

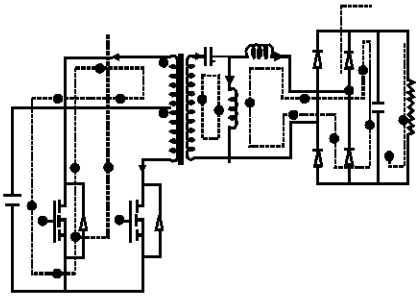

Fig. 3. (a) Mode 2

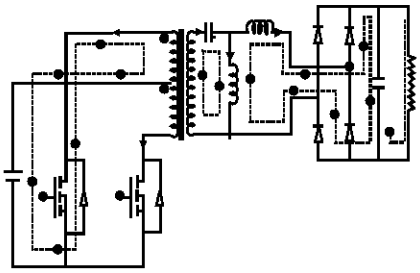

Fig. 3. (a) Mode 3

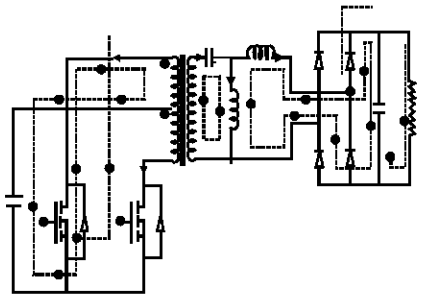

Fig. 3. (a) Mode 4

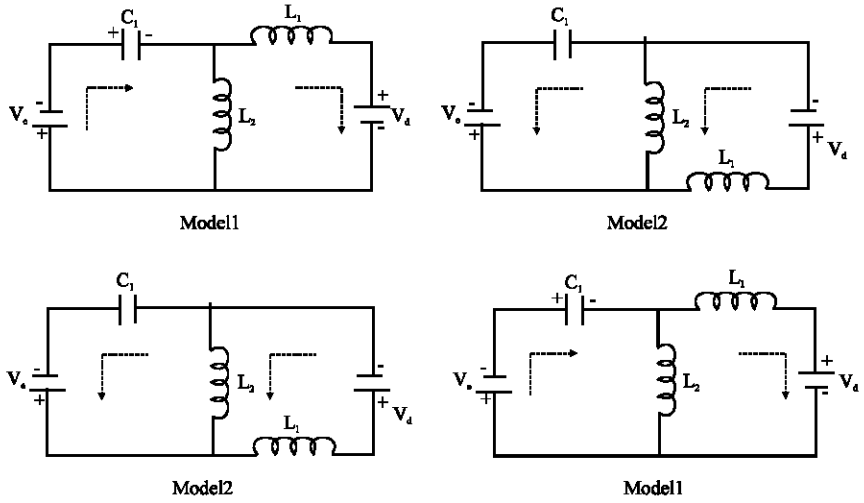

Fig. 3(b): Equivalent Circuit Model for each Mode

Mode 3

$$i_{C1}(t) = I_0 + (I_{C10} - I_0)\mathrm{Cos}(\omega_o t) + \left(\frac{(V_s + V_{L20})}{Z_4} - \frac{(V_s + V_d)}{Z_2}\right) \mathrm{Sin}(\omega_o t) + \frac{(V_s + V_d)}{Z_2}(\omega_o t)$$

$$I_0 = \left(\frac{(I_{C10}L_2 + L'I_{L10})}{L_2 + L'}\right)$$

$$i_{L1}(t) = I_0 + (I_{L10} + I_0)\mathrm{Cos}(\omega_o t) + \left(\frac{(V_{L20} - V_d)}{Z_1} + \frac{(V_s + V_d)}{Z_2}\right) \mathrm{Sin}(\omega_o t) - \frac{(V_s + V_d)}{Z_2}(\omega_o t)$$

$$V_{L2}(t) = V_0 + (V_{L20} - V_0)\mathrm{Cos}(\omega_o t) + (-I_{C10} - I_{L10})Z_3\mathrm{Sin}(\omega_o t)$$

$$V_0 = \left(\frac{L_2 V_d - L'V_s)}{L_2 + L'}\right)$$

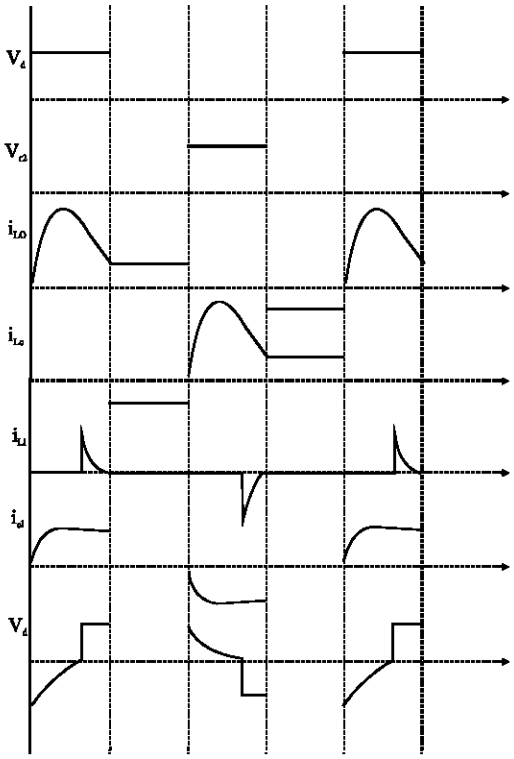

Fig. 4: Idealized waveform of CLL ZVCS resonant push-pull DC-DC Converter

Mode 4

$$i_{C1}(t) = I_0 + (I_{C10} - I_0)\mathrm{Cos}(\omega_o t) + \left(\frac{(V_s - V_{L20})}{Z_4} - \frac{(V_s - V_d)}{Z_2}\right)$$

$$\mathrm{Sin}(\omega_o t) + \frac{(V_s - V_d)}{Z_2}(\omega_o t)$$

$$I_0 = \left(\frac{(I_{C10}L_2 + L'I_{L10})}{L_2 + L'}\right)$$

$$i_{L1}(t) = -I_0 + (I_{L10} - I_0)\mathrm{Cos}(\omega_o t) + \left(\frac{(V_{L20} - V_d)}{Z_1} + \frac{(V_s - V_d)}{Z_2}\right)$$

$$\mathrm{Sin}(\omega_o t) - \frac{(V_s - V_d)}{Z_2}(\omega_o t)$$

$$V_{L2}(t) = V_0 + (V_{L20} - V_0)\mathrm{Cos}(\omega_o t) + (I_{C10} - I_{L10})Z_3\mathrm{Sin}(\omega_o t)$$

$$V_0 = \left(\frac{L_2 V_d - L'V_s)}{L_2 + L'}\right)$$

Where for each mode

$$L_1 + L_2 = L'$$

$$\omega_0 = j\sqrt{\frac{L'}{CL_1L_2}}$$

$$Z_1 = j\sqrt{\frac{L'L_1}{CL_2}}$$

$$Z_2 = j\left(1 - \frac{L'}{L_2}\right)\sqrt{\frac{L_1L_2}{CL'}}$$

$$Z_3 = j\sqrt{\frac{L'L_2}{CL_1}}$$

$$Z_4 = j\sqrt{\frac{L_1L_2}{L'C}}$$

CONVERTER SIMULATIONS

In this study the general purpose Pspice A/D has been used to simulate the new ZVCS CLL Resonant push-pull DC-DC converter. The CLL Resonant push-pull DC-. DCconverter circuit using Pspice software is shown in the Fig. 5. The open loop simulated waveforms of gating pulses of switches M_1 and M_2, current through capacitor C_1 and L_1 are shown in Fig. 6-8. The voltage across the rectifier input is shown in Fig. 9. The output voltage waveform is shown in Fig. 10. The simulated waveforms are closely agreed with the theoretical waveforms.

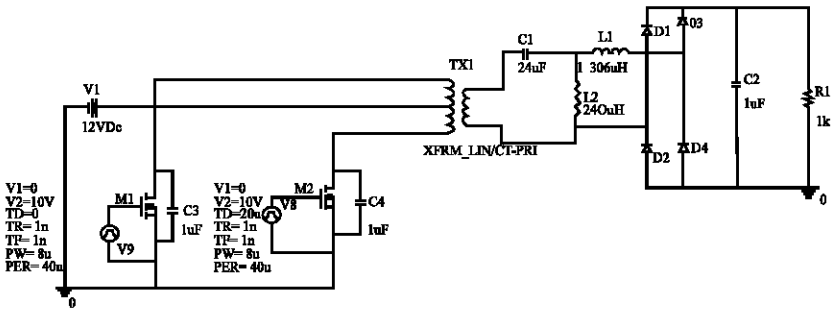

Fig. 5: CLL Resonant push-pull DC-DC converter

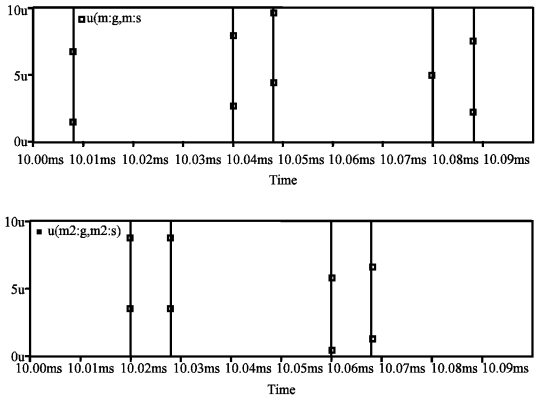

Fig. 6: Gating pulses of switches M_1 and M_2

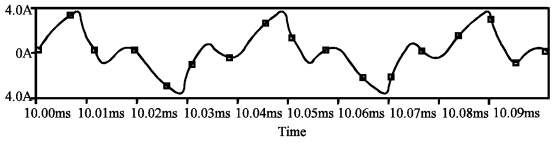

Fig. 7: Resonant Capacitor current (C_1)

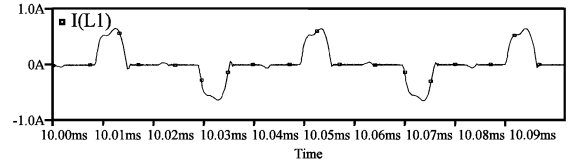

Fig. 8: Resonant inductor current (L_1)

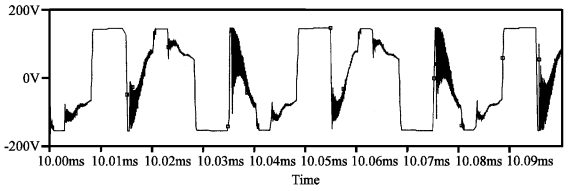

Fig. 9: Voltage across the rectifier input

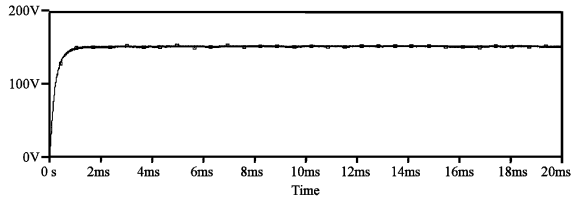

Fig. 10: Output voltage

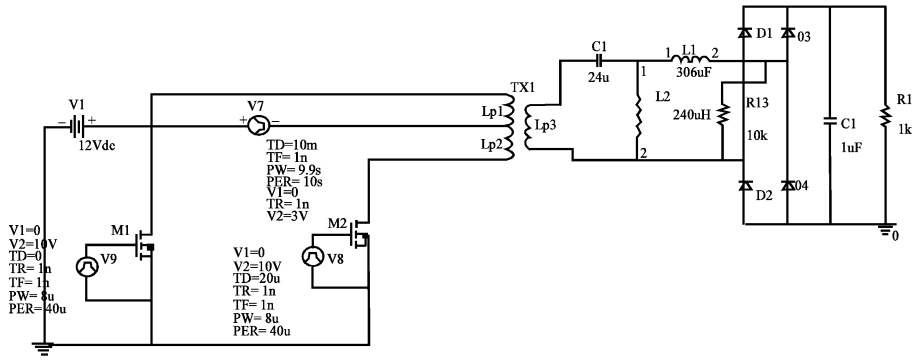

Fig. 11: CLL Resonant push-pull DC-DC Converter with disturbance

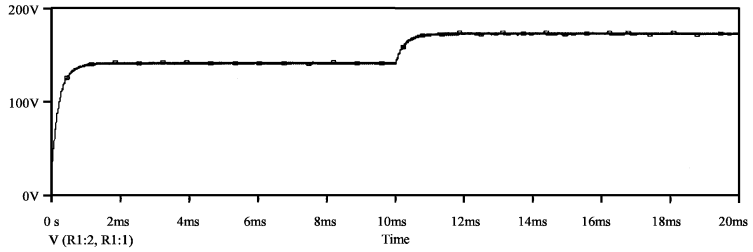

Fig. 12: Output voltage with disturbance

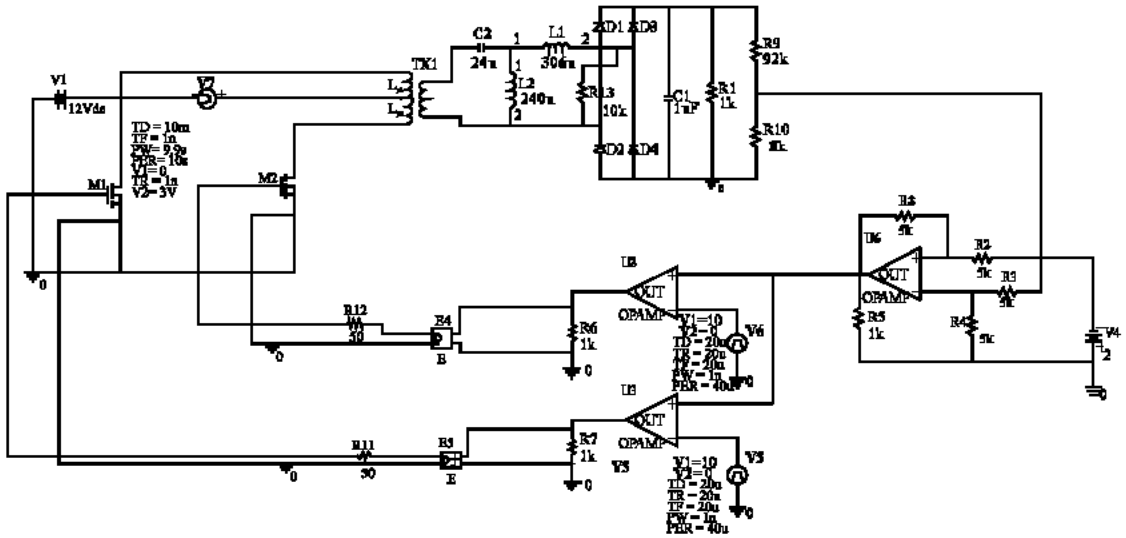

Fig. 13: Closed loop CLL Resonant push-pull DC-DC Converter

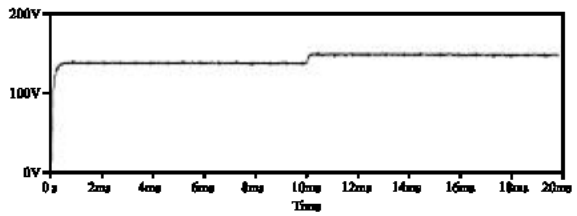

Fig. 14: Output voltage

The open-loop CLL Resonant push-pull DC-DC converter system with disturbance at the input side is shown in the Fig. 11. The output voltage waveform with disturbance is shown in Fig. 12. It can be seen that the output voltage waveform is disturbed at 10ms, due to the application of disturbance at the input side.

CLOSED LOOP SYSTEM

The output voltage of the converter changes when supply voltage is disturbed. A closed loop control system is therefore required to maintain the output voltage constant. A voltage proportional to the output voltage is compared with the reference voltage and PWM controller processes the error voltage obtained.

The ZVCS CLL Resonant push-pull DC-DC converter circuit in closed loop is shown in Fig. 13. The closed loop simulated waveform of output voltage is shown in Fig. 14. The output voltage remains almost constant.

The total harmonic distortion of ZVCS CLL Resonant push-pull DC-DC converter, for various values of resonant components are tabulated in Table 1.

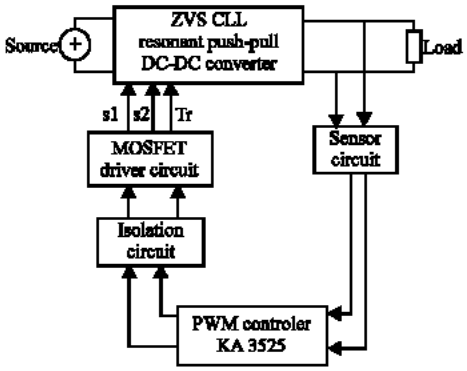

Fig. 15: Block diagram of CLL resonant push-pull DC-DC converter

Table 1: Various values of resonant components

S.No	L_1 µH	L_2 µH	C_1 µF	THD %
1	18	27	1	106.7
2	240	306	1	84.55
3	240	306	24	76.74
4	240	306	100	82.13

RESULTS

A Laboratory model of ZVS CLL-Resonant push-pull DC-DC Converter is implemented with the following specifications:

Input voltage (V_i) = 9.2v
Output voltage (V_o) = 10v
Output current (I_o) = 2A
Switching frequency (f_s) = 25kHz
Resonant frequency (f_r) = 50kHz
Resonant Inductor (L_1) = 0.16mH
Resonant inductor (L_2) = 0.16mH
Resonant capacitor (C_1) = 0.02 µf
Output Capacitor (C_2) = 1 µf

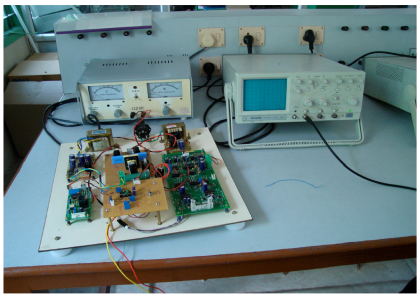

Fig. 16: Experimental set up of DC-DC converter

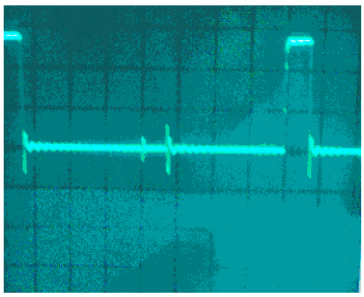

Fig. 17: Switching pulse volt div^{-1} 5V, time div^{-1} 5 μs

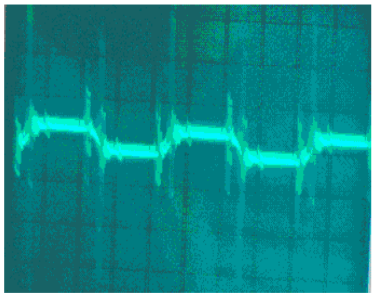

Fig. 18: Resonant capacitor voltage volt div^{-1} 0.5V, time div^{-1} 10 μs

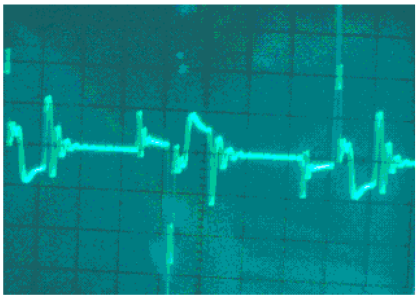

Fig. 19: Resonant inductor voltage volt div^{-1} 10V, time div^{-1} 5 μs

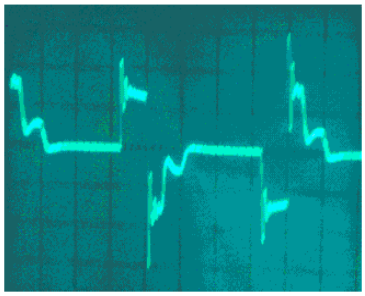

Fig. 20: Resonant Inductor Voltage Volt div^{-1} 10V, Time div^{-1} 5 μs

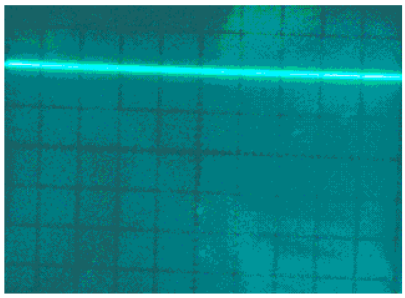

Fig. 21: Output voltage volt div^{-1} 5V, time div^{-1} 10 μs

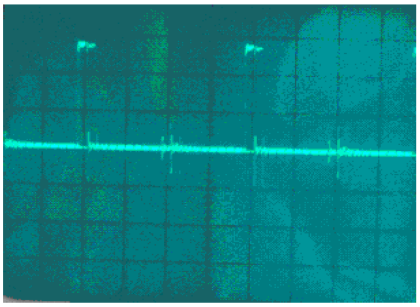

Fig. 22: Switching pulse volt div^{-1} 5V, time div^{-1}10 μs

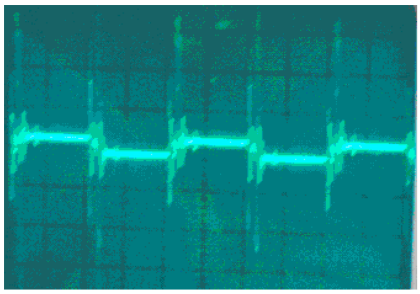

Fig. 23: Resonant capacitor voltage volt div^{-1} 5V, time div^{-1}10 μs

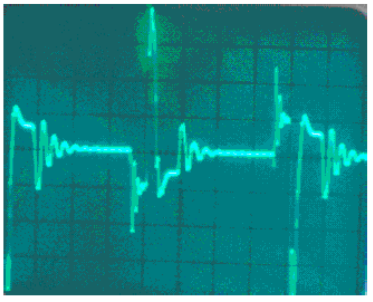

Fig. 24: Resonant Inductor Voltage Volt div^{-1} 10V, Time div^{-1} 5 μs

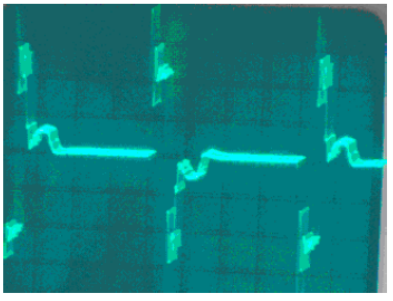

Fig. 25: Resonant Inductor voltage Volt div^{-1} 10V, Time div^{-1} 5 μs

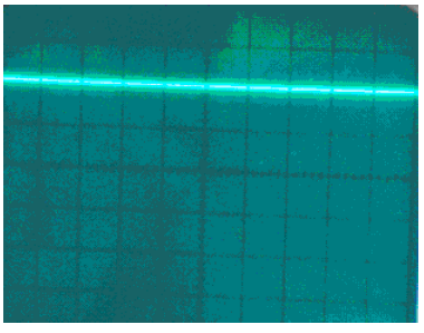

Fig. 26: Output voltage Volt div^{-1} 5V, Time div^{-1} 50 μs

The block diagram of the proposed converter is shown in Fig. 15.

The gating signals for MOSFET switches S_1 and S_2 are generated using PWM controller IC KA3525. The PWM controller IC compares the output voltage with reference voltage and produces the error voltage. The error voltage is compared with the reference triangular voltage and the gating signals for MOSFET switches S_1 and S_2 are generated.

The experimental setup of ZVS CLL Resonant push-pull DC-DC converter is shown in Fig. 16. The switching pulse is shown in Fig. 17. The resonant capacitor voltage in open loop condition is shown in Fig. 18. The resonant inductor voltage is shown in Fig. 19 and 20. The output voltage is shown in Fig. 21. The experimental waveforms closely agree with the simulated waveforms.

Table 2: The output voltage changes whenever the input voltage changes

		Open loop output voltage (V)	
Sl. No.	Input voltage (V)	T = 3 μs, D = 7.5%	T = 10 μs, D = 25%
1	4	4	6.5
2	5	5.2	8.2
3	6	6.5	9.6
4	7	7.5	11.2
5	8	8.7	12.8
6	9.2 v	10 v	14.5
7	10	11.0	15.75
8	11	12.1	17
9	12	13.3	18.3
10	13	14.4	19.5
11	14	15.5	20.2
12	16	17.7	22.5
13	18	20.1	24.7
14	20	22.3	27
15	25	-	30.7

Table 3: The input and output voltages for closed loop operation

Sl. No.	Input voltage (V)	Closed loop output voltage (V)
1	4	6
2	5	8.24
3	6	8.98
4	7	9.68
5	8	9.75
6	9	9.86
7	10	9.92
8	11	9.99
9	12	10.0
10	13	10.01
11	14	10.04
12	16	10.07
13	18	10.09
14	20	10.10
15	25	10.13
16	30	10.16

The output voltage changes whenever the input voltage changes. For various input values the corresponding converter output voltages are noted. The values are tabulated in Table 2.

Depending upon the error signal the PWM controller adjust the pulse width given to the MOSFET switches in order to maintain the output voltage as constant. The switching pulse is shown in Fig. 22. From the switching pulse it can be seen that the duty ratio of the PWM signal changes in order to maintain the output voltage constant. The resonant capacitor voltage is shown in Fig. 23. The resonant Inductor voltage is shown in Fig. 24 and 25. The output voltage is shown in Fig. 26. The input and output voltages for closed loop operation are tabulated in Table 3.

CONCLUSION

A new ZVCS resonant converter topology can operates at high-conversion efficiency and very low

switching noise with simple operation and low cost. It is ideally suited for unregulated DC- DC conversion from low voltage high-current source.

It is easily to control the output ripple voltage because most of the resonant current flow through the output capacitor. The open loop and closed loop operation of the ZVS-CLL Resonant push-pull DC- DC converter are simulated. The harmonic distortion of the converter is analyzed.

REFERENCES

Batarsed, I., 1994. Resonant converter topologies with three and four energy storage elements, IEEE. Trans. Power Electron, 9: 64-73.

Bo, Y., Y. Ren and F.C. Lee, 2002. Integrated magnetic for LLC resonant converter, IEEE. APEC. Proceed., pp: 346-351.

Bo Yang, F.C. Lee, J.A. Zhang and G. Huang, 2002. LLC resonant converter for front end DC-DC Conversion, IEEE. APEC. Proceed., pp: 1108-1112.

Boonvaroonote and S. Mori, 2002. A new ZVCS Resonant Push-Pull dc-dc Converter Topology: In Proceed. IEEE. Applied Power Elect. Conf. Exposit., pp: 1097.

Elferich, R. and T. Duerbaum, 2002. A New load resonant Dual output converter, Proc. IEEE. PESC., pp: 1319-1324.

Generalized topologies for converters with reactive energy storage, 1989. In conf. Rec. IEEE-IAS Ann. Meeting, pp: 1147-1151.

Lazar, J.F. and R. Martinelli, 2001. Steady State Analysis of the LLC series Resonant Converter, Proc. IEEE. APEC., pp: 728-735.

Liu, R. and C.Q. Lee, 1992. Series Resonant converter with Third order commutation Network, IEEE. Trans. Power Elect., pp: 462-467.

Liu, K.H. and F.C. Lee, 1986. Zero voltage switching technique in DC-DC Converter, In Conf. Rec. IEEE. PESC., 7: 58-70.

Ryan, M.J., W.E. Brumsickle, D.M. Divan and R.D. Lorenz, 1995. A new ZVS LCL-Resonant push-pull DC-DC converter topology, IEEE. Trans. Indus. Application, 34: 1164-1174.

Severns, R.P., 1992. Topologies for three-element resonant converters, IEEE. Trans. Power Elect., pp: 89-93.

Shoyama, M. and K. Harada, 1991. Zero voltage-switching realized by magnetizing current of transformer in push-pull DC-DC converter: In Proc. INTELEC., pp: 640-647.