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Analysis, Simulation and Development of Resonant Converter for DC Motor Drive System

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Abstract: The higher the frequency, better the waveform subject to certain limitation. However, with high load current, particularly when the switches are turned on and off they are subjected to high voltage stresses and high di/dt values. Due to this the power losses in the switches are high, which depends upon the frequency of modulation. In the recent years, attempts have been made to design the converter topology and improve the control strategies, so that switches are turned on and off while the current through it and/or voltage across it is zero. In order to achieve this condition LC circuits have been used in such away that the voltage and current pass through zero crossing due to resonance of LC circuits. Due to the advantages of high frequency of operation, higher efficiency, smaller size, lightweight, low component stresses and reduced electromagnetic interference there is an increased interest in the area of resonant converters. Various configurations of converter operation of LC resonance have been reported. One such configuration, which has number of desirable features, is known as series-parallel resonant converter. In this study, analysis of resonant converter has been carried out and the results predicted by the Pspice simulation are validated by the experimental results.

Key words: Zero voltage switching, zero voltage switching, dc-dc converter, resonant converter, soft switching

INTRODUCTION

The basic theoretical analysis for series connection of semiconductor power switches for zero voltage switching (Edson, 2000). In all pulse width modulated dc to dc and dc to ac converters, the controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching in this switched mode operation, the switches are subjected to high switching stresses and high switching power losses, that increase linearly with the switching frequency of PWM (Vijay and Seshagiri, 1998). Another significant draw back of switch mode operation is the EMI produced by large di/dt and dv/dt caused by switched mode operation (Rajapandian and Ned, 2001).

These shortcoming of switched mode converter can be over come if the switching frequency is increased in order to reduce the converter size and weight and hence to increase the power density (Gerry and Praveen, 1999). Therefore, to realize high switching frequencies in converters the aforementioned shortcomings are minimized if each switch in converter changes its status (from on to off and vice versa) when voltage across it and/or current through it is zero at the switching instant (Evandro and Antonio, 2004). The voltage and current are forced to pass through zero crossing by creating an LC resonant tank circuit, there by called resonant converters (Jose, 2004). This loss less zero-voltage scheme improves the performance characteristics (Ganesh *et al*., 1998). The equivalent circuit method simplifies the analysis and design of parallel and series-parallel resonant dc-dc converters loaded by a capacitive output filter (Gregory *et al*., 1999). These techniques allow operation at higher switching frequencies resulting in higher power densities without penalizing the efficiency (Carlos *et al*., 2000).

MATERIALS AND METHODS

L-type zcs resonant converters: An L-type ZCS resonant converter is shown in Fig.1: The switching device S in the diagram can be a GTO, thyristor, BJT, Power MOSFET or IGBT. At low kilohertz range; GTO, thyristor, transistor or IGBT is used whereas for megahertz range, power MOSFETs are preferred. Inductor L and Capacitor C near the dc source Vs form a resonant circuit whereas L_1, C_1 near the load constitute a filter circuit. Directions of currents and polarities of voltages as marked in the diagram are treated as positive. This employs a soft turn off technique.

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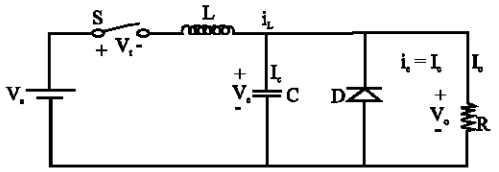

Fig. 1: L-Type ZCS resonant converter

An LC resonant circuit and appropriate control circuit ensure that the device is turned off when the inductor current goes to zero. This results ideally in zero turn-off losses.

The circuit is initially in the steady state with constant load current Io. Filter inductor L_1 is relatively large to assume that current i_o in L_1 is almost constant at Io. Initially, switch S is open; resonant circuit parameters have $i_L = 0$ in the $v_c = 0$ across C and the load current Io freewheels through the diode D.

For the sake of convenience, working of this converter is divided into 5 modes as under. For all these modes, time t is taken as zero at the beginning of each mode. To analyze its steady-state behavior, the following assumptions are made.

- Filter inductance is much larger than resonant inductance.
- Output filter and load are treated together as a constant current sink.
- Semiconductor switches are ideal (i.e.) no forward voltage drops in the on-state no leakage currents in the off-state and no time delays during both turn-on and turn-off.
- Reactive elements of the tank circuit are idea.

Mode I. ($0 \le t \le t_1$): At t = 0, switch S is turned on. As Io is freewheeling through diode D, voltage across ideal diode $v_d = 0$ and also $v_c = 0$ (Fig. 2a). It implies that source voltage Vs gets applied across L and the switch current i_L begins to flow through V_s, switch S, L and diode D, (Fig. 2a). Therefore, Vs = L di/dt. It gives $i_L = (Vs\ L^{-1})\ t$. It shows that inductor or switch current i_L rises linearly from its zero initial value. The diode current i_D is given by Eq. 1,

$$i_D = I_o - i_L = Io - (V_s / L)\ t \qquad (1)$$

At $t = t_1$, $i_L = (V_s / L)\ t_1 = Io$. This gives $t_1 = (I_o.L)$ /Vs.Also, at $t = t_1$, $i_D = I_o - I_o = 0$. Soon after i_1 , as i_D tends to reverse , diode D gets turned off, As a result of this , short circuits across C is removed (Fig. 3).

Mode II.($0 \le t \le t_2$): Switch S remains on. As D turns off at t = 0, current Io flows through V_s, L, L1 and R. In Fig. 2 (a and b), constant current through L_1 and R is represented by current source Io. Also, a current i_c begins to build up through resonant circuit consisting of Vs, L and C in series. The inductor current i_L is, Therefore,, given by Eq. 2

$$i_L = I_o + i_c = I_o + I_m \sin \omega_o t \qquad (2)$$

Where $Im = Vs\sqrt{(C/L)} = Vs/Zo$ and $\omega_o = 1/\sqrt{(LC)}$. Here $Z_o = \sqrt{(L / C)}$ is the characteristics impedance of the resonant circuit.

The capacitor voltage v_c is given by Eq. 3,

$$v_c (t) = V_s (1 - \cos \omega_o t) \qquad (3)$$

The peak value of current i_L is $I_p = I_o + I_m$ and it occurs at, $t = (\pi / 2\omega_o) = (\pi/2)\sqrt{(LC)}$. At this instant, $v_c (t) = Vs (1 - \cos \pi) = 2V_s$ and $i_c = I_m$. When $t = t_2 = \pi/\omega_o = \pi\sqrt{(LC)}$, capacitor voltage reaches peak value $V_{cp} = Vs (1 - \cos \pi) = 2Vs$ and $i_c = 0$. Also at $t = t_2$, $i_L = I_o$, i.e. switch current drops from peak value (Io + Im) to Io.

Mode III ($0 \le t \le t_3$): Switch S remains on. At t = 0, capacitor voltage is 2Vs. As i_c tends to reverse at t = 0, capacitor begins to discharge and force a current $i_c = Vs\ \sqrt{(C/ L)} \sin \omega_o t$ opposite to i_L, (Fig. 2c) , so that inductor or device current i_L is given by Eq. 4,

$$i_L = I_o - i_c = I_o - I_m \sin \omega_o t \qquad (4)$$

And capacitor voltage $v_c = 2V_s \cos \omega_o t$. Current i_L falls to zero when $t = t_3$,i.e., $i_L = 0 = Io - Im \sin \omega_o t$ Or $t_3 = \sqrt{(LC)}$ $\sin^{-1} (Io / I_m)$. During this mode, $i_c = Im \sin \omega_o t$ and as i_L falls to zero at t_3 , switching device S gets turned off . Note that current i_c in this mode flows opposite to its positive direction, it is Therefore, shown negative in Fig. 2c. At $t = t_3$, the value of $i_c = -I_o$.

Mode IV ($0 \le t \le t_4$): As switch S is turned of at t = 0, capacitor begins to supply the load current Io as shown in Fig. 2d. Capacitor voltage at any time t is given by Eq. 5,

$$v_c = V_{c3} - (1/C) \int i_c \, . \, dt \qquad (5)$$

As magnitude of capacitor current i_c = Io is constant,$v_c = V_{c3} - (Io/C)t$. This mode comes to an end when v_c falls to zero at $t = t_4$, or $0 = V_{c3} - (Io/C)\ t_4$ or $t_4 = C.V_{c3}/Io$. At t = 0, $v_T = Vs - V_{c3}$ and at $t = t_4$, $v_T = V_s - 0 = V_s$ as shown in Fig. 2d. As Io is constant, capacitor discharges linearly from V_{c3} to zero and v_T varies linearly from $(V_s - V_{c3})$ to V_s.

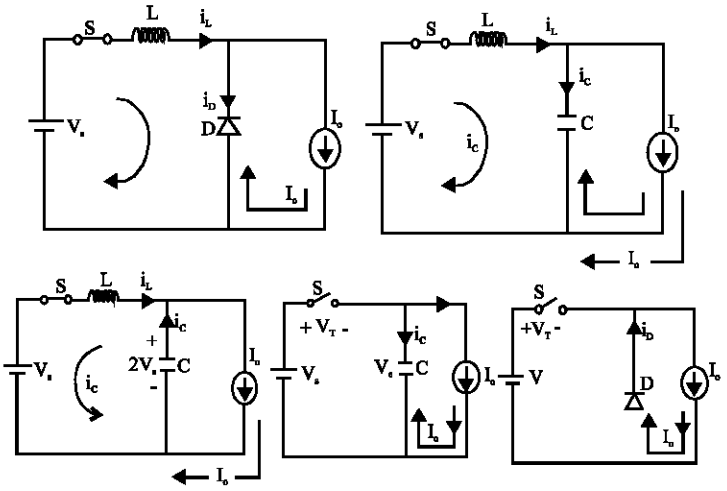

Fig. 2: Equivalent Circuits for the operating modes of L-type ZCS resonant converter (a) Mode I $i_D = I_o - i_L$ (b) Mode I $i_L = I_o + i_c$ (c) Mode III $i_L = I_o - i_C$ (d) Mode IV $-i_c = i_o$ (e) Mode V $i_D = I_o$

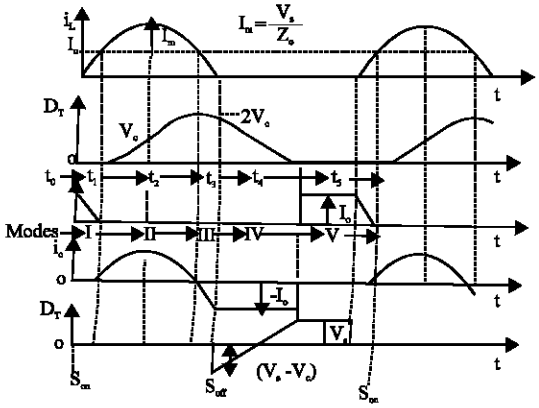

Fig. 3: Waveforms of L-type ZCS resonant converter

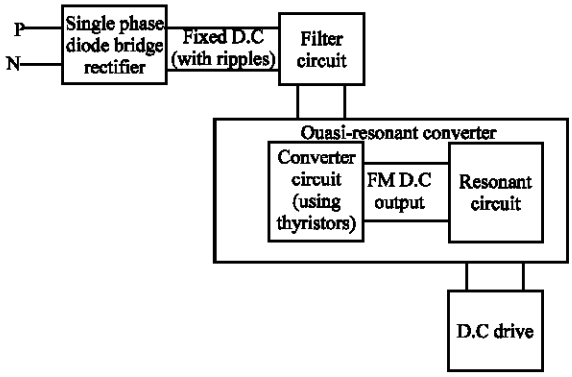

Fig. 4: Block diagram of QRC fed DC drive

Mode V ($0 \le t \le t_5$): At the end of mode IV or in the beginning of mode V, capacitor voltage v_c is zero. As v_c tends to reverse at t = 0, diode D gets forward biased and starts conducting, (Fig. 2e). The load current Io flows through the diode D so that id = Io during this mode. This mode comes to an end when switch S is again turned on at $t = t_5$. The cycle is now repeated as before. Here $t_5 = T - (t_1 + t_2 + t_3 + t_4)$.

The waveforms for switch or inductor current i_L, capacitor voltage v_L, diode current i_d, capacitor current i_c and voltage across switch S as v_T. It is seen that at turn-on at $t = 0$ ($0 \le t \le t_1$), switch current $i_L = 0$, Therefore, switching loss $v_L i_L = 0$. Similarly at turn-off at t_3 ($0 \le t \le t_3$), $i_L = 0$ and therefore, $v_L i_L = 0$. It shows that the switching loss during turn-on and turn-off processes is almost zero. The peak resonant current Im = (Vs/Zo) must be more than the load current Io, otherwise switch current i_L will not fall to zero and switch S will nor get turned off.

The load voltage v_o can be regulated by varying the period t_5. It is obvious that longer the period t_5, lower is the load voltage.

BLOCK DIAGRAM

The single-phase AC supply is fed to a bridge rectifier circuit, which converts the input AC. Signal into fixed DC signal with ripples. Then this fixed DC signal with ripples is fed to a filter circuit to filter out the ripples. The free DC signal is fed to a quasi-resonant converter. The quasi-resonant converter consists of a converter circuit (consists of thyristors) and resonant circuit (consists of inductor and capacitor). When this ripple free DC signal is given as the input to the converter, we get frequency modulated DC output. When this FM modulated DC output is passed through the resonant circuit, we get a quasi-resonated frequency

modulated DC output. This frequency modulated, quasi-resonated DC output is fed to the load (DC. motor) and its speed can be controlled effectively and efficiently (Fig. 4).

POWER CIRCUIT

The power circuit consists of, Step down transformer, Bridge rectifier, Filter circuit, SCR, Quasi-resonantcircuit, Free wheeling diode, DC. Motor.

The single phase, 220V, AC. supply is given to a step-down transformer whose rating is 220V/18V as shown in Fig. 5. So the output of the transformer is 18V (AC). This stepped down AC. voltage is given as input to a bridge rectifier (formed with the help of IN4001 diodes), which converts the given AC. signal in to an AC. one.

The output from the rectifier circuit (DC) consists of ripples and in order to reduce/suppress it, it is fed to a filter circuit, which consists of an inductor and a capacitor whose values are 100mH and 1000uF/50V, respectively. To get the controlled DC voltage, the filtered wave is given to a SCR, which converts the uncontrolled DC. in to a controlled one. Then this controlled DC wave is fed to a LC tank circuit (resonant circuit, which is operated in quasi-resonant mode), which gives quasi-resonated output. Finally, this quasi-resonated output is fed to a DC drive through a freewheeling diode and thus the drive is effectively controlled to the required range. The combination of SCR, tank circuit and the freewheeling diode is called quasi-resonant converter.

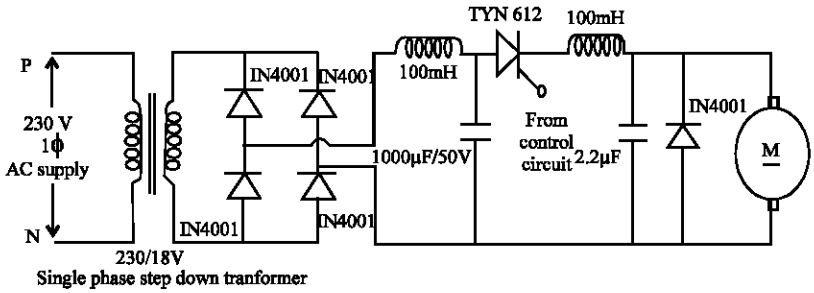

Fig. 5: Power circuit

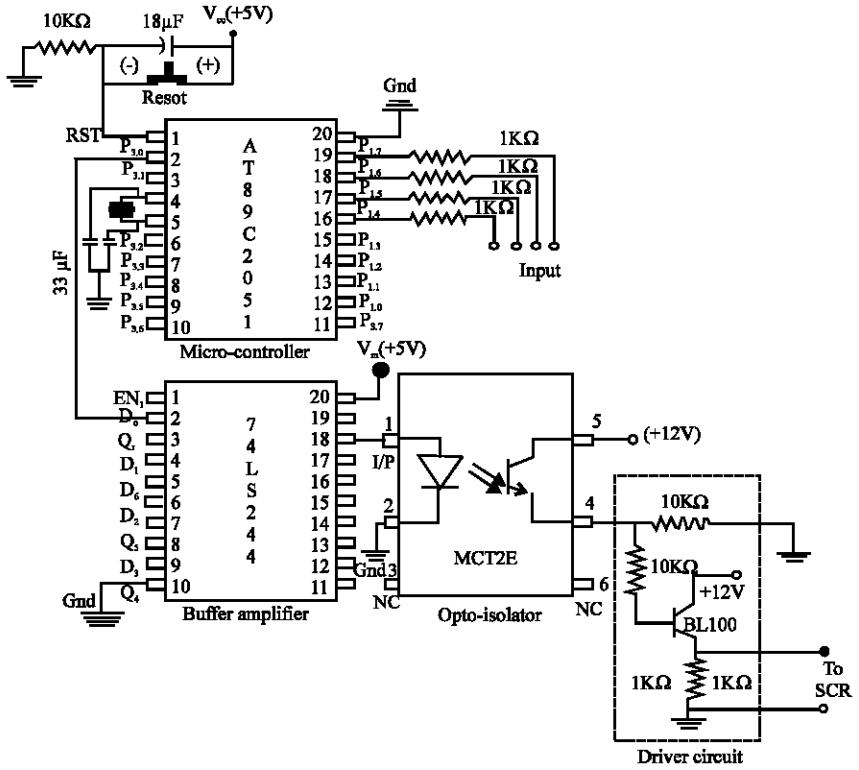

Fig. 6: Control circuit

CONTROL CIRCUIT

The control circuit of Fig. 6 consists of Micro-controller, Buffer Amplifier, Opto- isolator, Driver circuit. The OFF time of SCR is given as the input to the micro-controller via., thumbwheel switch. According to the input delay time, the micro-controller generates control signal (Fig. 7 and 8).

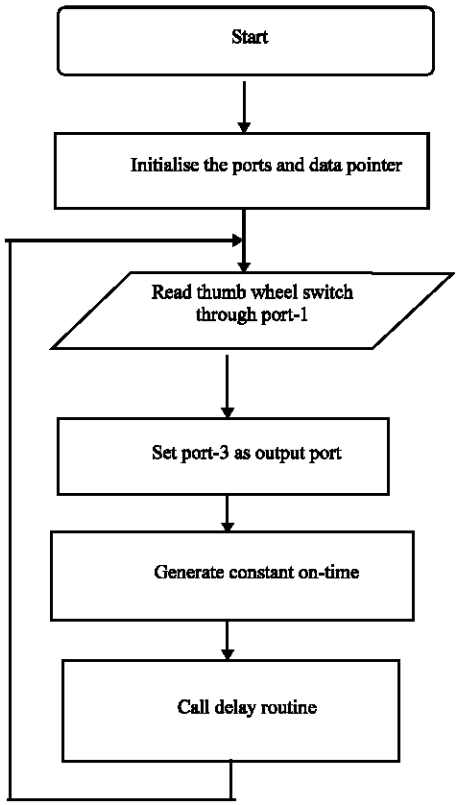

Fig. 7: Main routine

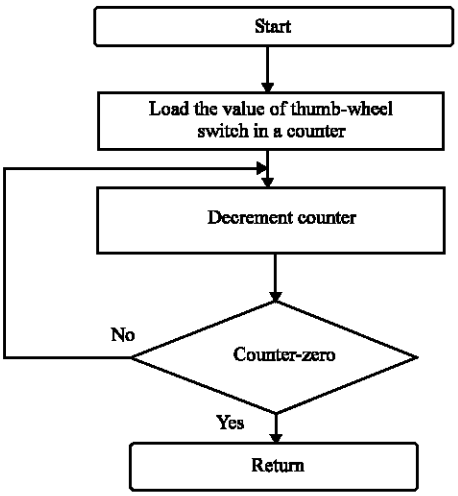

Fig. 8: Delay routine

The output from the micro-controller is insufficient in magnitude to trigger the gate of the SCR. Hence the output has to be amplified with the help of buffer amplifier. The output from buffer amplifier is fed to opto-isolator. The isolation between power circuit and control circuit is obtained with the help of opto-isolator.The output from the opto-isolator is fed to the gate-cathode of SCR through a driver circuit.

Program

```
P1 EQU 90H
DPL EQU 82H
DPH EQU 83H
P3 EQU 0B0H

ORG 0000H
MOV P1, #0FFH
MOV P3, #00H
MOV DPTR, #0100H

KK:     SET B P3.0
MOV R0, #0FFH
EE:         DJNZ R0, EE
MOV A, P1
CPL A
SWAP A
ANL A, #0FH
MOVC A, @A+DPTR
MOV R1, A
CLR P3.0
DD:     MOV R2, #0FFH
AA:     DJNZ R2, AA
DJNZ R1, DD
SJMP KK
ORG 0100H]
DB05H, 10H, 5H, 20H, 25H, 30H, 35H, 40H, 45H, 50H
```

RESULTS AND DISCUSSION

The hardware and software aspects of the QRC fed DC drive system are discussed in detail. This study explains the results of QRC system and the conclusion drawn there from. A FM-ZCS-QRC has been constructed and used successfully to control the speed of a separately excited dc motor. Speed control of the motor was accomplished by varying the dead time (TOFF) of the QRC.The efficiency of QRC fed dc

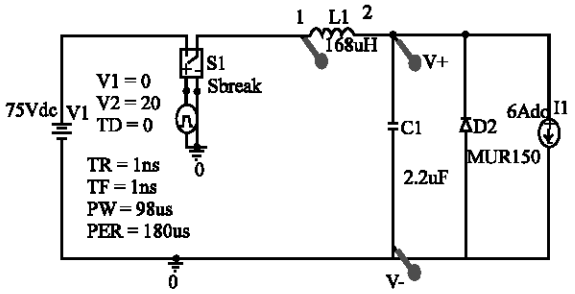

Fig. 9: Simulation circuit for FM-ZCS-QRC (Half wave mode)

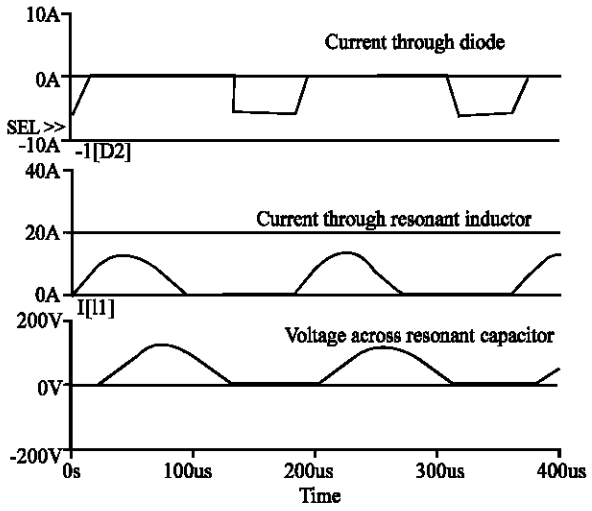

Fig. 10: Simulated output result for FM - ZCS – QRC (Half wave mode)

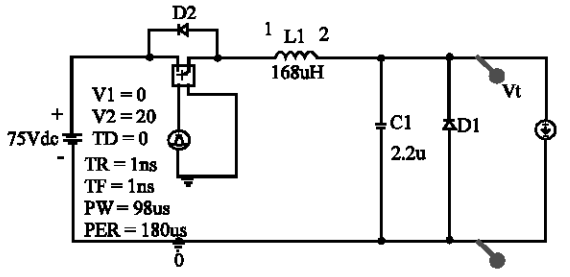

Fig. 11: Simulation circuit for series QRC (Full Wave Mode)

drive has been found to be better than that of conventional drives. This is a consequence of soft switching which considerably reduces the switching losses shown in Fig. 9-16.

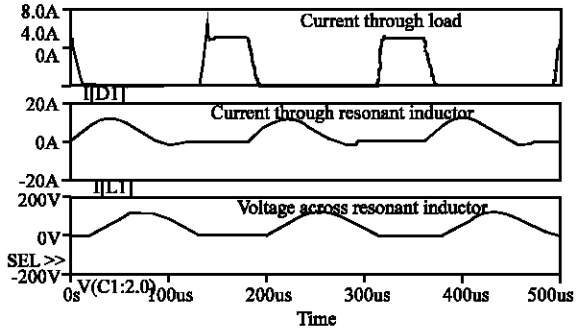

Fig. 12: Simulation output for SERIES QRC (full wave mode)

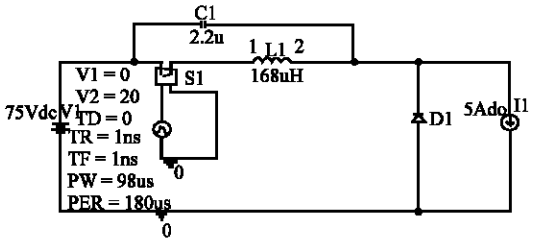

Fig. 13: Simulation circuit for parallel QRC (half wave mode)

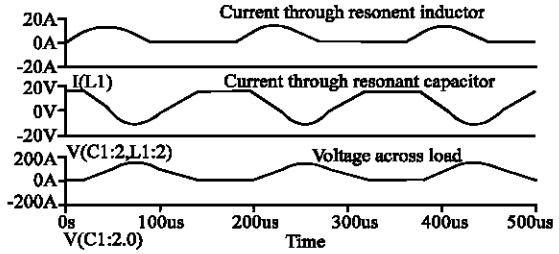

Fig. 14: Simulation output for parallel QRC (half wave mode)

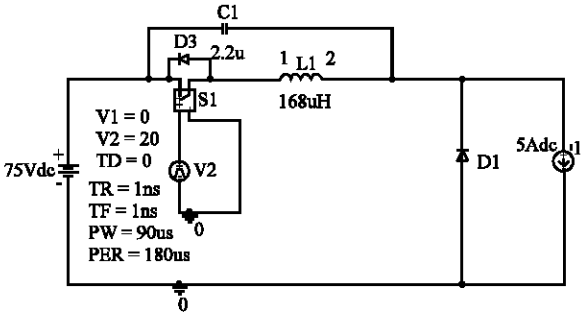

Fig. 15: Simulation circuit for parallel QRC (full wave mode)

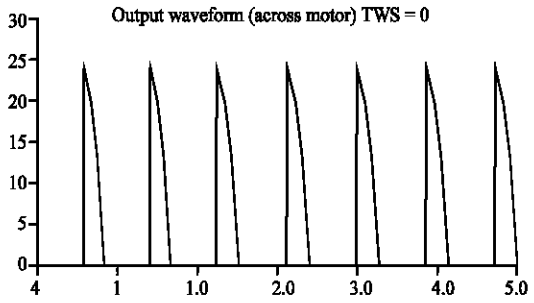

Fig. 16: Experimental output for SERIES QRC (Full Wave Mode)

CONCLUSION

QRCs have been found to enjoy many advantages like improved efficiency, higher reliability and reduced hardware. Hence the application of QRCs to the dc drives has promising future. The disadvantages are the derating of the machine and the requirement of devices with higher voltage rating.

NOTATIONS

FM : Frequency Modulation.
ZCS : Zero Current Switching.
QRC : Quasi-Resonant Converter.
PWM : Pulse Width Modulation.
V_{in} : Input AC voltage.
D : Diode.
D_f : Freewheeling diode.
L_f : Filter inductor.
C_f : Filter Capacitor.
L_r : Resonant inductor.
C_r : Resonant capacitor.
I_a : Armature current.

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