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Voltage Sag Mitigation in Multi-Line Transmission System Using GUPFC

[1]T. Ruban Deva Prakash and [2]N. Kesavan Nair
[1]Sathyabama University, Chennai, India
[2]N.I College of Engineering, Kumarakoil, India

Abstract: Voltage sag is one of the most severe power quality disturbances to be dealt with by the industrial sector, as it can cause severe process disruptions and result in substantial economic loss. One of the main factors which limit capabilities of Dynamic Voltage Restorer (DVR) in compensating long-duration voltage sags is the amount of stored energy within the restorer. In order to overcome this limitation, Inter-line Dynamic Voltage Restorer (IDVR) has been proposed where two DVRs each compensating a transmission line by series voltage injection, connected with common dc-link. When one DVR compensates voltage sag, the other DVR of the IDVR replenish the dc-link energy storage. This IDVR works efficiently when the lines under consideration are connected with two different grid substations, as it is reasonable to assume that voltage sag in one line would have lesser impact on the other line. But in case when the lines are connected with same grid substation and feeding two different sensitive loads in an industrial park, voltage sag in one line affects the voltage profile of other lines. Under the above circumstances, long duration voltage sags cannot be mitigated by IDVR due to insufficient energy storage in dc-link. This study proposes a voltage sag compensator based on Generalized Unified Power Flow Controller (GUPFC), which comprises of three voltage-sourced converter modules sharing a common dc link. Two voltage-sourced converter modules connected in series with the lines, which compensates voltage sag and a third shunt converter module maintains bus voltage and replenish the common dc-link energy storage. The control strategy for power flow control of shunt converter and sag compensation control of series converters are discussed in detail. Adjustable carrier PWM is used for generating switching pulses. The simulation model of GUPFC is developed in this study. The salient advantages of the proposed method are compensating long duration deeper voltage sags, reduction in size of dc-link capacitor and simultaneous voltage sag compensation in all lines. Simulation results presented for a simple system under three-phase voltage sag of 40% and -20° phase angle jump demonstrates the efficiency of the proposed system.

Key words: Voltage sag, DVR, IDVR, GUPFC, adjustable carrier PWM

INTRODUCTION

Voltage deviation often in the form of voltage sag is one of the most severe power quality disturbances. Even short duration voltage sag could cause a malfunction or a failure of a continuous process, thereby incurring heavy financial loss. A series connected converter based mitigation device, the Dynamic Voltage Restorer (DVR) proposed by Woodley *et al.* (1999) is the most economical and technically advanced mitigation device proposed to protect sensitive loads from voltage sags. The amount of energy storage within the DVR becomes one of the main limiting factors in mitigating long duration voltage sags. Therefore, researchers presently pay greater attention to the DVR energy storage and its optimum use. A new circuit topology in which the DVR energy storage is dynamically replenished by means of a front-end controllable rectifier has been proposed by Vilathgamuwa and Wijekoon (2002). A progressive phase advance technique where all the three phase voltages are progressively advanced by a certain angle to minimize the amount of real power supplied by the DVR has been proposed by Vilathgamuwa *et al.* (1999) and Li *et al.* (2000).

Mahinda *et al.* (2004) presented a concept of Interline Dynamic Voltage Restoration (IDVR) where two or more voltage restorers are connected such a way that they share a common dc link. This is similar to Interline Power Flow Controller (IPFC) explained by Gyugyi *et al.* (1999) which is still under research for the compensation and effective power flow management of multi-line transmission system. In IDVR system, two different sensitive loads in an industrial park fed from two different feeders with different voltage levels can be protected

Corresponding Author: N. Kesavan Nair, 54, Anjali Nager, Pettah, Pallimukku, Thiruvananthapuram-695024, Kerala, India

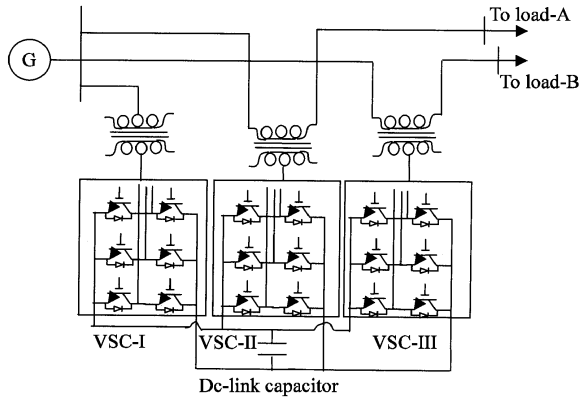

Fig. 1: Basic connection of GUPFC

from voltage sags by two DVRs having common dc link. This would cut down the cost of the custom power device, as sharing a common dc link reduces the dc link storage capacity significantly compared to that of a system whose loads are protected by clusters of DVRs with separate energy storages.

In modern power system a simple radial system may not be considered suitable for certain concentrated loads as it has the least reliability. Settembrini *et al.* (1991) stated that, the distribution systems such as secondary selective systems are common nowadays in industrial plants and institutions where the customer load is generally divided between the two feeders. The IDVR system works well, when both the feeders are fed from two different substations, as voltage sag in one feeder may not have any influence on the other feeder. Hence, when one DVR in a feeder compensates voltage sag, the DVR in the other feeder replenish the dc link energy storage. But in case when the feeders are in parallel and fed from the same substation, the voltage sags in one feeder causes voltage sag in the other feeder also. Thus both the DVRs of IDVR system should compensate for voltage sag and there is no way to replenish the DC link energy storage. Thus IDVR system fails to mitigate long duration deep voltage sags.

This study proposes a compensating device based on the concept of generalized UPFC. This concept is illustrated in Fig. 1. It comprises of three standard voltage sourced converter module sharing a common dc link. Two voltage sourced converter module are connected in series to the lines in parallel and can regulate the real and reactive power flow through the lines. The third converter module is connected in shunt with the bus, which can regulate the dc link voltage. Thus, the two series converter module can compensate voltage sag simultaneously in both lines, whereas the shunt converter module replenishes the dc link energy storage. This device injects three single-phase voltages in series with the incoming supply voltages. The magnitude and phase angle of the injected voltage can vary depending on the sag parameters. The voltage injection creates variable real and reactive power exchange between the compensating device and the sensitive load of the distribution system. The amount of real and reactive power supplied by the GUPFC depends on the type of voltage disturbances, the protected load and the magnitude and direction of injected voltage. The reactive power can be internally generated within the GUPFC, while energy storage is required to supply the real power. Holmes and McGrath (2001) proved that the switching signal generation technique used for the switches of an electronic converter influences its ability to obtain the desired objectives. The injected voltage of this device depends on the accuracy and dynamic behavior of the Pulse Width Modulated (PWM) voltage synthesis scheme adopted. Hence this study uses a novel switching signal generation technique called Adjustable Carrier PWM (ACPWM) proposed by Cadaval *et al.* (2005) which guarantees that the supply currents follow the reference currents determined by the compensation strategy, with the smallest possible RMS tracking error. The steady state operation of IPFC is explained by Diez-Valencia *et al.* (2002) which presents mathematical model of IPFC. The Generalized Unified Power Flow Controller (GUPFC) is introduced by Zhang (2002) which explains its modeling in Newton power flow. Using those basic concepts, this study presents a simulation model of GUPFC.

The control strategy adopted for generating reference signal plays a key role in deciding the dynamic behavior of a system. Usually, the control voltage for mitigating voltage sag is derived by comparing the supply voltage against a reference waveform as explained by Nielsen *et al.* (2001). Although the system stability is guaranteed in this type of control, the stability margin can be inadequate and the damping of output voltage would be poor. Because of these reasons, the current mode feedback control proposed by Vilathgamuwa *et al.* (2002) is gaining acceptance for voltage sag mitigation. The GUPFC is similar to Generalized IPFC (GIPFC), but the converter modules of GIPFC have separate DC links.

The GUPFC has an additional shunt converter module sharing common DC link along with an IPFC module. The basic control of IPFC is explained by Chen *et al.* (2002). Due to approximation in the process of the control design the control scheme presented by Chen has some tracking error. Hence, this study presents control schemes for voltage sag compensation of series converters and power flow control of shunt converter. Simulation results are presented for a simple system in order to demonstrate the efficiency of the proposed system.

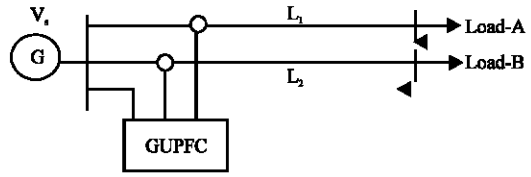

Fig. 2: Basic connection of GUPFC

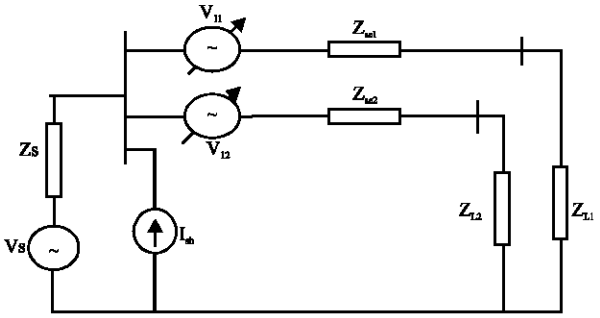

Fig. 3: System model

SYSTEM MODEL

Figure 2 shows the single line diagram of a system which has two transmission lines L_1 and L_2 which feeds load A and B respectively. The GUPFC is installed near the sending-end bus in the system. The circuit model is shown in Fig. 3. The series converter modules of GUPFC connected to the transmission line are modeled as variable voltage sources V_{11} and V_{12}. The shunt converter module is modeled as current source I_{sh}. The series impedance of the lines is represented as Z_{sc1} and Z_{sc2}. The impedance of the loads is denoted as Z_{L1} and Z_{L2}. The source voltage is V_s and its impedance is Z_s.

The shunt converter module is controlled such a way to maintain dc link voltage and bus voltage at a desired level. In this study, the bus voltage control is not incorporated for simplicity. This control is referred as power flow control mode. The series converter modules are controlled such a way to mitigate voltage sag. The control strategies are explained in the following section.

POWER FLOW CONTROL STRATEGY

In this mode, the dc link voltage is maintained constant by using the shunt converter module of the GUPFC. A simple control algorithm is developed which does not use PI controller. To regulate the dc link capacitor voltage at the desired level, an additional real power has to be drawn by the GUPFC from the supply side to charge the two capacitors. The energy 'E' stored in each capacitor can be reprinted as

$$E = \tfrac{1}{2}C\left[\frac{V_{dc}}{2}\right]^2 \quad (1)$$

Where 'C' is the value of each capacitor and $V_{dc}/2$ is the voltage of each capacitor.

If the desired level of voltage across each capacitor is $V_{dc(ref)}/2$, the energy for capacitor is

$$E^{l} = \tfrac{1}{2}C\left[\frac{V_{dc(ref)}}{2}\right]^2 \quad (2)$$

The difference between E' and E represents the additional energy required by capacitor to reach the desired voltage level. Thus

$$\Delta E = E^{l} - E = \tfrac{1}{2}C\left\{\left[\frac{V_{dc(ref)}}{2}\right]^2 - \left[\frac{V_{dc}}{2}\right]^2\right\} \quad (3)$$

On the other hand, the charging energy E_{ac} delivered by the three phase supply side to the inventor of each capacitor will be

$$\begin{aligned} E_{ac} &= 3pt \\ &= 3(E_{rms} I_{dc(rms)} \cos\Phi)t. \end{aligned} \quad (4)$$

P - Additional real power required
V_{rms}- RMS value of the instantaneous supply voltage
$I_{de(rms)}$- RMS value of the instantaneous charging current.
ϕ - Phase deference between the supply voltage and charging current
t - Charging time.

Here't' can be defined as T, where 'T' is the period of supply frequency. By using Phase Lock Loop (PLL) the charging current is made in phase with the supply voltage and hence $\cos\phi = 1$. Also the RMS value can be expressed in terms of maximum values.
This result in

$$E_{ac} = 3\frac{V}{\sqrt{2}}\frac{I_{dc}}{\sqrt{2}}T. \quad (5)$$

$$E_{ac} = \frac{3VI_{dc}T}{2} \quad (6)$$

Neglecting the switching losses in the inverter and according to the energy conservation law the following equation holds $\Delta E = E_{ac}$.

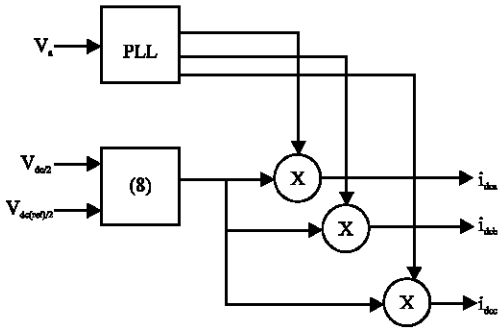

Fig. 4: Three-phase self charging circuit

$$\frac{1}{2}C=\left\{\left[\frac{V_{dc(ref)}}{2}\right]^2-\left[\frac{V_{dc}}{2}\right]^2\right\}=\frac{3VI_{dc}T}{4} \quad (7)$$

$$I_{dc}=2C\frac{\left\{\left[V_{dc}(ref)\right]^2-\left[V_{dc}\right]^2\right\}}{3VT} \quad (8)$$

The configuration of three – phase self charging current is shown in Fig. 4. The PLL synchronizes itself with the supply voltage of phase 'a' and outputs three sine waves which are 120° out of phase from each other. These sine waves are multiplied with I_{dc} to obtain the three phase i_{dc}. Thus the three phase injection currents can be calculated as

$$\begin{aligned} i_{inj,a} &= -I_{dc}\sin\omega t \\ i_{inj,b} &= -I_{dc}\sin(\omega t-120) \\ i_{inj,c} &= -I_{dc}\sin(\omega t+120) \end{aligned} \quad (9)$$

The minus sign indicates that the charging current i_{dc} flows into the GUPFC. An adjustable carrier PWM controller is used to control the switching of the GUPFC.

VOLTAGE SAG COMPENSATION CONTROL STRATEGY

The commonly used basic voltage sag compensation techniques are In-phase boosting technique, Pre-sag supply voltage boosting technique and energy optimum boosting technique. The simplest pre-sag supply voltage boosting technique is considered for developing a new two neuron control algorithm. The pre-sag voltage boosting technique can be explained by vector diagram shown in Fig. 5.

Current is taken as reference vector throughout this section. Under pre-sag condition, the system voltage is V_{t-1} which leads current by an angle φ. At time't', sag occurs in supply voltage and is shifted in phase by an

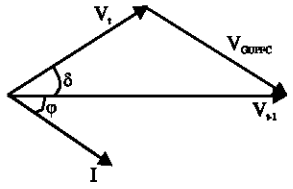

Fig. 5: Vector diagram for pre-sag supply voltage boosting technique

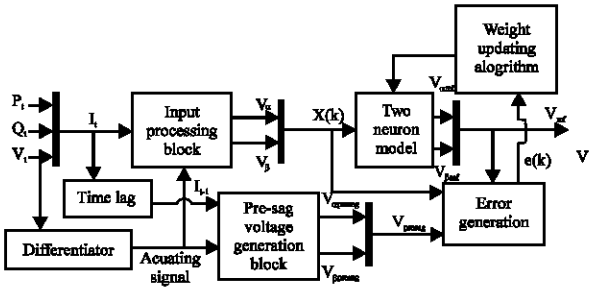

Fig. 6: Basic block diagram of proposed controller

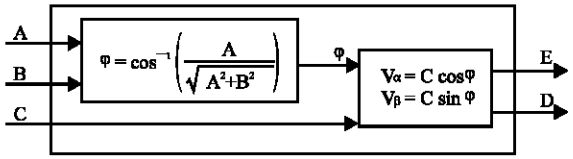

Fig. 7: Input processing/pre-sag voltage generation block

angle δ called phase angle jump. The ratio of voltage during sag to voltage before sag is referred as sag factor 'a'. That is, $a = V_t/V_{t-1}$. The series converter of GUPFC has to inject a voltage 'V_{GUPFC}' such a way to bring voltage during sag V_t to its pre-sag value V_{t-1}. The control algorithm developed for generating the reference signal to compensate voltage sag is named as two-neuron control technology. The control law is given as $V_{\alpha ref} = \gamma_1 V_\alpha$ and $V_{\beta ref} = \gamma_2 V_\beta$, where γ_1 and γ_2 are constants which are interpreted weights in the two-neuron model. $V_{\alpha ref}$ and $V_{\beta ref}$ denote the components of reference voltage in-phase and in phase-quadrature with line current, respectively. The magnitude and angle of reference voltage can be calculated as,

$$|V|_{ref}=\sqrt{V_{\alpha ref}^2+V_{\beta ref}^2} \quad (10)$$

$$\theta_{ref}=\tan^{-1}\left(\frac{V_{\beta ref}}{V_{\alpha ref}}\right) \quad (11)$$

The basic block diagram of the control algorithm is shown in Fig. 6.

The input processing block and pre-sag voltage generation block performs the same function of

calculating the in-phase and phase-quadrature components of voltage, but for different input quantities. Figure 7 shows the input processing/pre-sag voltage generation block. In case of input processing function, the inputs and outputs are A=P_t ; B=Q_t; C=V_t ; D=V_α and E=$V_{\hat{a}}$. On the other hand, for pre-sag voltage generation the inputs and outputs are A=P_{t-1}; B=Q_{t-1}; C=V_{t-1}; D=$V_{\alpha presag}$ and E=$V_{\hat{a}presag}$. The time lag block in Fig. 6 is used for obtaining inputs P_{t-1}, Q_{t-1} and V_{t-1} from P_t, Q_t and V_t respectively. The inputs are denoted in figure as.

$$I_t = \left[P_t, Q_t, |V_t|\right] \text{ and } I_{t-1} = \left[P_{t-1}, Q_{t-1}, |V_{t-1}|\right]$$

Both input processing block and pre-sag voltage generation block responds to input only when activating signal is generated by the differentiator (Fig. 6). Under normal condition without voltage sag, the differentiator output is zero and the blocks are not activated.

The error generator block is shown in Fig. 8. The line voltage is added with reference voltage generated by the control algorithm and compared with the pre-sag voltage generated by pre-sag voltage generation block. The error signal is given as input to weight updating algorithm.
The error is given by

$$e(k) = \begin{bmatrix} V_{\alpha e} \\ V_{\beta e} \end{bmatrix} \tag{12}$$

The weight updating algorithm uses delta rule to update the weights of the two-neuron model. The weight vector is

$$W(k) = \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \tag{13}$$

The delta rule used for updating weights is

$$W(k+1) = W(k) + \frac{\alpha e(k) X(k)}{\lambda + X(k) X(k)^T} \tag{14}$$

Where α is the reduction factor, λ is a constant chosen to be close to zero and is included only to avoid division by zero and X(k) is the input vector of the two-neuron model given as,

$$X(k) = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{15}$$

The two-neuron model is shown in Fig. 9, which has two neurons and the activity of neuron is finding the product of input (V_α and $V_{\hat{a}}$) and weight (γ_1 and γ_2).

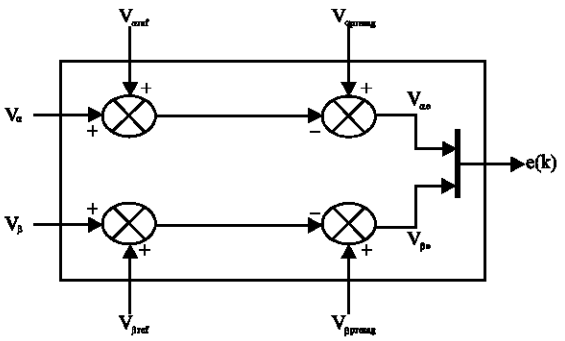

Fig. 8: Error generator

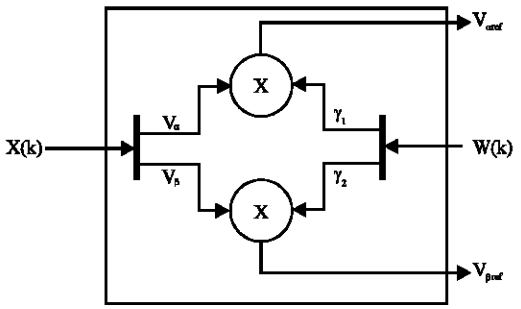

Fig. 9: Two-Neuron model

ADJUSTABLE CARRIER PWM

ACPWM uses two possible carrier signals in each sample period 'T_s', which are a rising toothed wave and a falling toothed wave. The wave which is used depends on the sign of the error. If the error is positive, the rising wave is used and if the error is negative, the falling wave is used. Thus the switching period will be T_s or $2T_s$ depending on the sign of the error. Assuming a uniform distribution for the error, an average switching frequency can be defined as $f_{c,med} = 3/4\ f_{ts}$, where, f_{ts} is the frequency of the toothed saw wave. The RMS tracking error of current can be minimized using this conditional wave.

SIMULATION STUDIES

A detailed simulation has been carried out for a simple GUPFC system consisting of two lines of 6.6 KV. The parameters of GUPFC system are given in Table 1. Two lines are feeding equal loads of 1MVA with 0.8 PF lagging. Simulation results presented in this study are for a three-phase voltage sag of 40% and phase angle jump of -20° appearing in the load bus of line L_2. Phase-A of the supply voltage of lines L_1 and L_2 are shown in Fig. 10 (a) and (b). The effect of sag in line L_2 is pronounced in line L_1 also. The series converter of GUPFC connected with lines L_1 and L_2 are operated in voltage sag compensating

Table 1: Parameters of the two-line GUPFC system

Parameter	Values
Supply voltage per phase (KV)	3.81
Load resistance (Ω)	35.0
Load inductance (mH)	83.0
Transformer resistance (Ω)	0.05
Transformer leakage inductance (mH)	1.0
Filter resistance (Ω)	0.05
Filter inductance (mH)	10.0
Filter capacitance (μF)	86
Common dc-link capacitance (μF)	14400

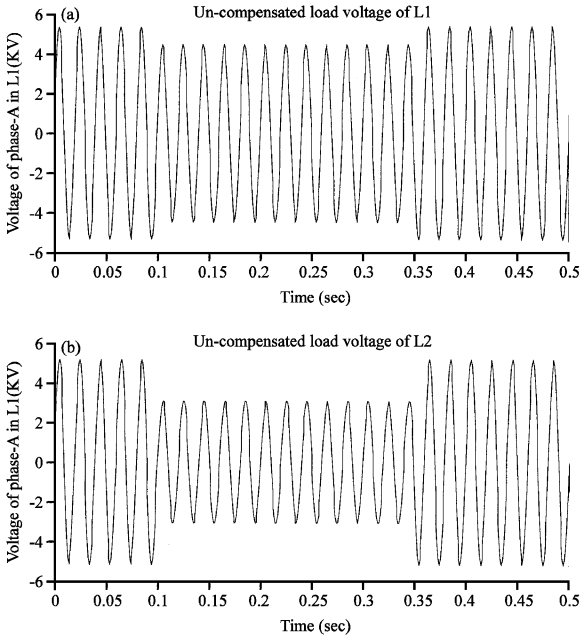

Fig. 10: Uncompensated load voltage of lines L_1 and L_2

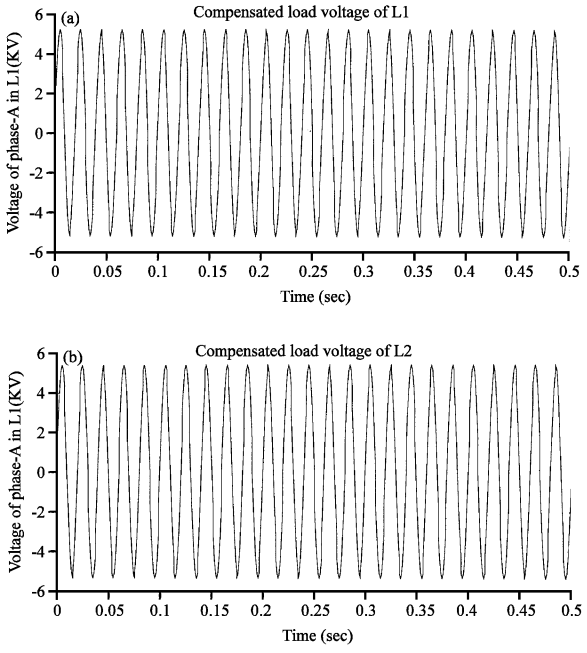

Fig. 11: Compensated load voltage of lines L_1 and L_2

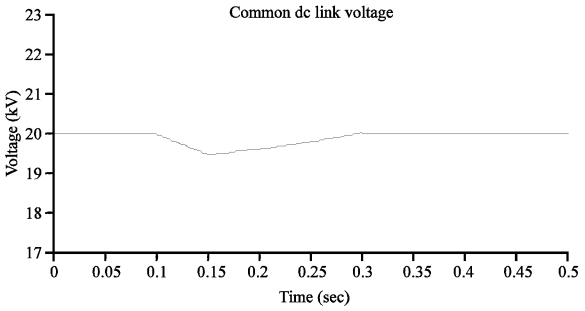

Fig. 12: Common dc-link voltage

mode. The compensated load voltage of lines L_1 and L_2 in Fig. 11 shows that the load voltage tracks the desired reference accurately without RMS tracking error under ACPWM. It also proves the effectiveness of the two-neuron control technology for voltage sag compensation. The degree of damping and dynamic performances is within the acceptable limits. The shunt converter is operated in power flow control mode which replenishes the dc-link energy storage. The dc-link voltage is presented in Fig. 12, which shows an initial drop at the start of GUPFC to compensate voltage sag and is brought towards reference within a short time. The initial drop is due to sudden power change in line L_1 and initially, this power is supplied from the dc-link energy storage and the shunt controller takes a certain time to react to the change in energy. Thus the overall performance of the proposed method is satisfactory.

CONCLUSION

The capability of any device used to compensate long duration voltage sag mainly depends on the amount of energy stored within the device. Moreover, the existing compensating devices cannot compensate simultaneously all the lines under consideration. This study has proposed a new concept of using GUPFC in voltage sag mitigation which can minimize the dc link energy storage, as well as, performs simultaneous compensation of all lines under consideration. Simulation results proved the efficiency of the proposed method. In the existing IDVR system, the amount of real power that a line can transfer to dc-link energy storage depends on the load PF. The proposed approach overcomes this limitation also. Thus this approach is a valuable contribution to the supply system in maintaining power quality. In future, this research can be extended for compensating more than two lines simultaneously.

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