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Implementing Built-In Test in Analog and Mixed-Signal Embedded-Core-Based System-On-Chips

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Abstract: This study aims to develop an approach to test analog and mixed-signal embedded-core-based sSystem-On-Chips (SOCs) with built-in hardware. In particular, Oscillation-Based built-In Self-Test (OBIST) methodology for testing analog components in mixed-signal circuits is implemented in this study. The proposed OBIST structure is utilized for on-chip generation of oscillatory responses corresponding to the analog-circuit components. A major advantage of the OBIST method is that it does not require stimulus generators or complex response analyzers which makes it suitable for testing analog circuits in mixed-signal SOC environments. Extensive simulation results on sample analog and mixed-signal benchmark circuits and other circuits described by netlist in HSPICE format are provided to demonstrate the feasibility, usefulness and relevance of the proposed implementations.

Key words: Embedded-core-based system-on-chips, testing, self-test, oscillation-based methodology, analog systems, mixed-signal systems, fault model, test procedure

INTRODUCTION

Ever increasing applications of the analog and mixed-signal embedded-core-based System-On-Chips (SOCs) (Rajsuman, 2000), in recent years have motivated system designers and test engineers to shift their research direction to embrace this particular area of very large-scale integrated circuits and systems to develop specifically their effective test strategies. An important objective to realize through detailed testing is to ensure that the manufactured products are free from defects and to simultaneously guarantee that they meet all the required specifications. Besides, the information that may be acquired through the process may ultimately help in increasing the product yield, thereby reducing the product cost. The Integrated Circuit (IC) fabrication process involves photolithography, printing, etching and doping steps. In the real-world situations, none of these steps is ever perfect and the resulting imperfections may eventually lead to failures in the operation of the individual ICs. Specifically, the performance of mixed-signal ICs will be greatly degraded, since these circuits are very sensitive to even small imperfections in any step of the fabrication process. In the digital-circuit domain however, some of these may be rather unimportant but in mixed-signal circuits, imperfection in the form of small capacitance between the traces can present a significant circuit-parameter variation, thereby changing the circuit behavior drastically. Because of the shrinking of the circuit geometry, the circuit performance sensitivity is also enhanced (Rajsuman, 2000; Hurst, 1998; Burns and Roberts, 2001; Wagner and Williams, 1988; Soma and Kolarik, 1994; Vazquez *et al*., 1994; Arabi and Kaminska, 1996). Researchers are now seeking to combine both the analog and the digital-circuits testing either by applying digital signals, such as serial bit streams to drive analog circuits or by using analog signals to drive digital circuits. The test methodologies for digital devices are already pretty well developed (Wang and Wey, 1998).

MATERIALS AND METHODS

Mixed-signal ICS and OBIST: Process technology has allowed analog and mixed-signal designers to integrate notable amount of functionality of a system onto a single chip. In general, there are two types of SOCs, viz., one that has grown from the application-specific (Fig. 1).

IC (ASIC) world while the other emanated from the custom IC world. This kind of design is digital integration

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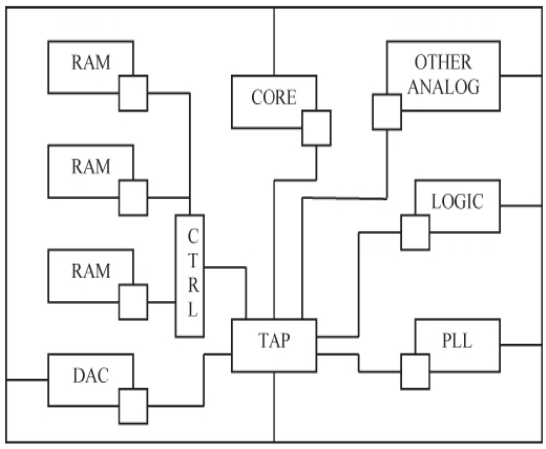

Fig. 1: Typical analog and mixed-signal SOC

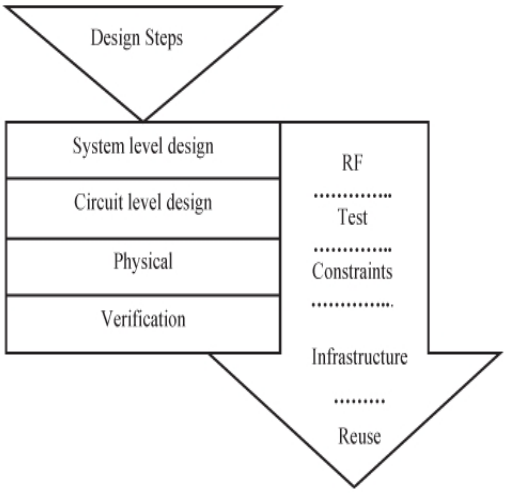

Fig. 2: Design flow of analog and mixed-signal SOCs

and it is interfaced with analog devices by embedded software. The analog and mitxed-signal blocks are integrated only when the time and cost spent on the integration are reasonable. The latter type of design, called analog and mixed-signal design, has high performance and complex signal paths through both the analog and the digital components. An example of mixed-signal SOC is illustrated by Fig. 2 where the main components tend to be a Digital-to-Analog Converter (DAC), Phase-Locked Loop (PLL), Random-Access Memory (RAM), logic and other cores. Figure 3 illustrates the design flow of analog and mixed-signal SOCs.

The procedure is such that a complex analog circuit is partitioned into functional building blocks such as Operational Amplifiers (Op Amps), comparators, filters, PLLs and so on or a combination of these blocks. Then, each building block is converted into an oscillator by

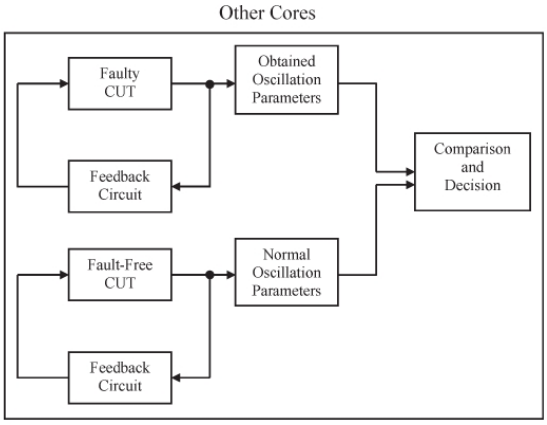

Fig. 3: Block diagram of OBT strategy

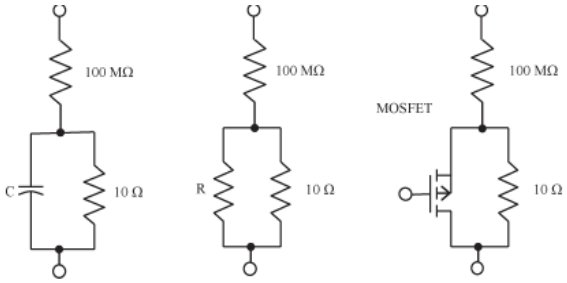

Fig. 4: Stuck-open and stuck-short fault models for capacitor, resistor and MOSFET

adding the proper circuitry in order to achieve sustained oscillation; the oscillation parameters are evaluated next. A faulty circuit is detected from a deviation of its oscillation parameters with respect to the oscillation parameters under fault-free conditions. In view of the fact that oscillation parameters are independent of the CUT type, analog testing can be standardized. Figure 4 shows a block diagram of the OBT strategy. The oscillation parameters can be the frequency, amplitude, distortion or dc level of the output signal. Although, this method provides high fault coverage by considering only the oscillation frequency, there may be some faults that may not be correlated with the frequency. In such cases, other test parameters have to be taken into consideration. For example, the fault coverage is improved by monitoring the supply current in addition to the oscillation frequency and output voltage.

To extract the oscillation parameters from the output test signals, a delta-sigma ($\Delta\Sigma$) modulator is connected to the output of the CUT to provide a train of modulated pulses that contain all the information about the output of the CUT. In order to extract the oscillation parameters, the train of pulses is processed using an Automatic Test

Equipment (ATE) or on-chip digital-signal processor. The implementation strategies for OBIST may vary based on the tradeoffs between the test time and the area overhead. The technique proposed in this study for testing analog and mixed-signal circuits based on OBIST is next explained in detail as follows.

Building an oscillator: Another way to design a sinusoidal oscillator from the transfer function is to connect the output terminal of the filter to the input terminal. The basic requirements for oscillation are a signal feedback from the output to the input of proper phase and sufficient amplitude. Some oscillators use RC elements for phasing. Some others operate on the principle of presenting a negative resistance as the feedback element. The design equations of an oscillator are determined by analyzing the denominator of the transfer equation T(s) of the circuit. The poles of the denominator of the characteristic equation T(s) or equivalently the zeros of T(s), determine the time-domain behavior and stability of the system . If the magnitude of the oop-gain is >1 and the phase is zero, the amplitude of oscillation will increase exponentially until a factor in the system, such as the supply voltage, restricts the growth. In contrast, if the magnitude of the loop-gain is <1, the amplitude of oscillation will exponentially decrease to zero.

Converting a filter into an oscillator requires a mechanism to force the placement of a pair of poles on the jω-axis. The general biquadratic transfer function is given by:

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + bls + b_0}$$

Where, $b_1 = \omega_0/Q$ and $b_0 = \omega_0^2$. The relation between the pole, pole frequency and quality factor is given by:

$$p_1 p_2 = \sigma \pm j\omega = -\frac{\omega_0}{2Q} \pm j\omega_0 \sqrt{1 + (\frac{1}{4Q^2})}$$

Where, ω_0 is the pole frequency and Q is the pole quality factor that determines the distance of the poles on jω-axis in the s-plane. An infinite Q locates the poles on the jω-axis and this can cause the circuit to oscillate. Therefore, in order for a filter to oscillate, the quality factor must be increased.

Fault model: Faults occurring in analog circuits can be categorized in two types: hard and soft faults. Hard faults or catastrophic faults are those faults that cause the circuit performance to differ catastrophically from normal conditions. Catastrophic fault model is the same as stuck-fault model used in the digital test domain where every component can be either stuck-open or stuck-short.

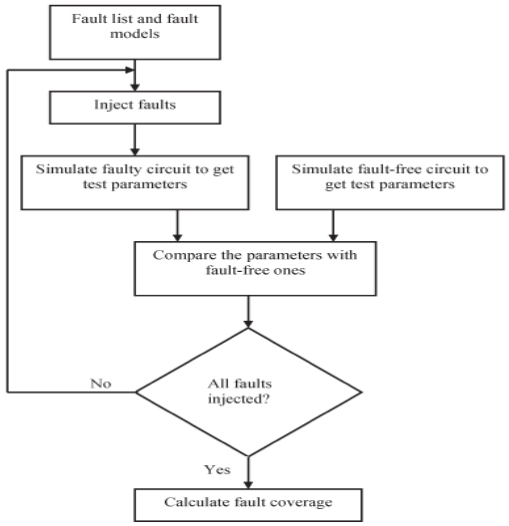

Fig. 5: Test procedure based on OBIST approach

Stuck-open fault results when the terminal of an analog circuit component is not connected to the rest of the circuit while stuck-short fault occurs when a short is created between the terminals of a component. On the other hand, soft or parametric faults refer to changes in a circuit that do not affect its connectivity, resulting in circuit functions out of specifications. The parametric faults can be modeled as variations of component parameters that are beyond their tolerance limits.

In this study, only catastrophic faults are considered. Figure 4 depicts standard fault models for capacitors, resistors and MOS Field-Effect Transistors (MOSFETs), where the value for the parallel resistor Rp is 10 MΩ that emulates stuck-short fault and that of the series resistor Rs has a value of 100 MΩ that emulates stuck-open fault. These fault models are used in HSPICE simulations in this study (Fig. 5).

RESULTS AND DISCUSSION

Test procedure: Purely analog ICs, unlike digital ICs, usually consist of relatively few circuit primitives such as amplifiers, comparators, etc. but many parameters must be considered for test. The test parameters are specified by designers and can be gain, offset voltage, slew rate, signal-to-noise ratio, bandwidth and so on. Traditionally, analog circuits have been tested functionally for specifications such as offset voltage, signal-to-noise

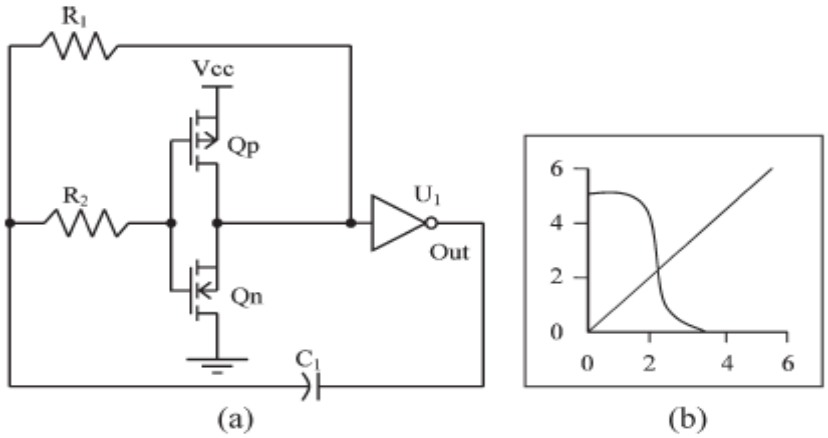

Fig. 6: a) Circuit; b) Transfer characteristics

ratio, etc. and functional test is still used in wafer level and packaged tests. This is primarily due to lack of any standard fault model for analog circuits.

In the application of the testing procedure proposed in this study, stuck-open and stuck-short faults are first injected at the circuit level. These faults are described in HSPICE format and are injected into nominal circuit descriptions. By using the HSPICE simulator, the transient response is then evaluated and frequency and output voltage are measured. Figure 6 gives a flow-chart representation of the test procedure based on OBIST approach. In the following, we provide an overview of the different steps of the procedure.

- Step 1: The fault-free circuit is converted into an oscillator and simulated and its test parameters (oscillation frequency and amplitude of the output signal) are derived
- Step 2: A fault list was derived from the CUT (circuit netlist)
- Step 3: The faulty netlist is generated (through fault injection
- Step 4: A simulation was done for the faulty CUT
- Step 5: The fault detection was completed on comparing the faulty-output measurements with fault-free test parameters
- Step 6: The procedure is continued until all faults are injected
- Step 7: The circuit fault coverage was calculated

The procedure is implemented using computer programs written in C programming language.

CONCLUSION

This study investigates the implementation of OBIST technique in testing analog parts in mixed-signal circuits. The OBIST method does not require stimulus generators or complex-response analyzers and has been gainfully employed in testing analog and mixed-signal circuits in embedded core- based SOC environments. The catastrophic faults are considered in this study and extensive simulation results on sample analog and mixed-signal benchmark circuits and other circuits are analyzed for fault-coverage evaluations, demonstrating that OBIST methodology does provide high-fault coverage with low-area overhead.

NOMENCLATURE

$V_o(s)$ = Output voltage
$V_i(s)$ = Input voltage
$H(s)$ = The transfer function of a continuous-time all-pole second order system
a_0-a_2 = Constants specifying the filter properties in terms of the basic filter
b_0-b_2 types of high pass, band pass and low pass, which occur when only one of the constants is nonzero. Combinations of these types create further filter types, such as notch and all pass filters
p_1, p_2 = Poles
Q = The q-factor
ω_0 = The angular frequency, $\omega_0 = 2\pi f_0$
f_0 = Frequency

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