Power Optimized Vedic Parallel MAC Unit: GDI Technique

[1]E. Prabhu and [2]H. Mangalam
[1]Department of Electronics and Communication Engineering, Amrita School of Engineering,
Amrita Vishwa Vidyapeetham University,
[2]Department of Electronics and Communication Engineering,
Sri Ramakrishna Institute of Technology, Coimbatore, India

Abstract: In vedic mathematics of the sixteen algorithms, Urdhva Tiryakbhyam is identified as one among the efficient algorithms for multiplication in terms of delay, power and area. In this study, a parallel MAC unit has been developed which employs compressor based Urdhva Tiryakbhyam multiplier for its operation. Transistor level power optimization is realized by Gate Diffusion Input (GDI) Technique using Synopsys HSPICE. The main advantage of the proposed technique is use of less number of transistors, result in reduced power consumption. The experimental results indicate an absolute reduction in total power consumption by 39 and 34.2% for 4-bit and 8-bit MAC, respectively when compared to standard CMOS technique.

Key words: Gate diffusion input, parallel MAC, vedic mathematics, modified GDI, low power

INTRODUCTION

The critical concern in the present VLSI system design is power consumption. Flying growth in portable electronic devices, demand for compact design, less power dissipation and increased speed activates countless research efforts. The desire to enhance the performance of logic circuits, traditionally based on standard CMOS technology, resulted in the growth of different logic design technologies. The most common form that is well accepted in low power digital circuits is Pass-Transistor Logic (PTL) where set of input is applied to gate and source NMOS transistor. Number of PTL design is already proposed in literatures. The focal benefit of PTL design over standard CMOS design are:

- Reduced transistor count which results in less power consumption
- Smaller area which results in lower interconnection effect
- Increased speed due to reduced nodal capacitance

However, there are two main problems associated with the PTL implementation. First, fall in threshold voltage across single channel pass transistor out-turns deceased current drive and reduced operation at slower supply voltage. This will be highly significant for low power design since, it is advantageous to operate at lowest possible voltage. Second problem, highest voltage level of NMOS is not 'VDD' and lowest voltage level of PMOS is not '0' hence, significant direct path power dissipation occurs. Different PTL implementations are proposed to solve above mentioned two basic problems.

CMOS-TG (Transmission Gate): In this logic by the usage of complementary transistors low level logic swing problem can be resolved. Complex logic function can be realized by using NMOS and PMOS transistors.

CPL (Complementary Pass transistor Logic): In this logic, complementary input and output by using NMOS pass-transistor with CMOS inverters. The logic has less power dissipation due to low internal node swing but have high static power consumption due to the reduced voltage swing at the gates of output inverters.

DPL (Double Pass-transistor Logic): In this logic both NMOS and PMOS transistor present. This method is used to overcome the threshold drop problem. It is advanced version of CPL logic that produce full output swing. The overall area increases due to the presence of PMOS logic.

The researches in MAC hardware mainly focus on enhancing its speed so as to achieve better performance. A high speed parallel MAC architecture was proposed in (Seo and Kim, 2010) based on modified booth algorithm. Recently, another high speed parallel MAC unit was

---

Corresponding Author: E. Prabhu, Department of Electronics and Communication Engineering,
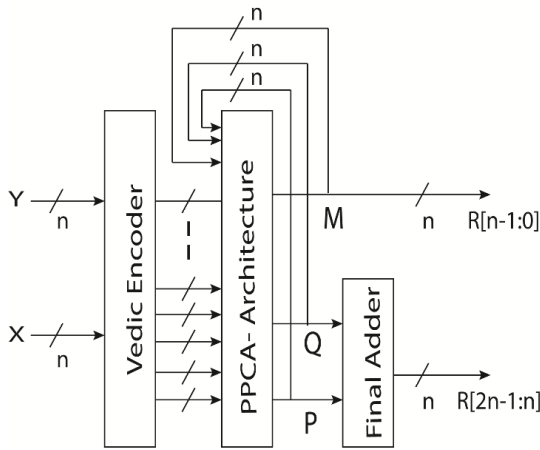Amrita School of Engineering, Amrita Vishwa Vidyapeetham University, Coimbatore, India

Fig. 1: Vedic parallel MAC architecture (Jithin and Prabhu, 2015)

proposed in (Jithin and Prabhu, 2015) based on vedic mathematics shown in Fig. 1. Sixteen simple sutras are discussed by Tirthaji (1986). The transistor level implementation of the parallel MAC is generally carried out by standard CMOS technology. Nevertheless by using GDI technique the overall power consumption of the circuit can be minimized substantially.

MATERIALS AND METHODS

Compressor adder: A compressor adder to improve overall computational speed of processor is designed (Chang *et al.*, 2004; Huddar *et al.*, 2013). A high speed 4:2 compressor is designed by Aliparast *et al.* (2011). About 20% improvement in speed can be achieved by using 4:2 compressors, instead of conventional full adders for 5 bit addition operation.

Gate diffusion input technique: A technology used for the design of less complexity digital circuits. The main advantage of this technique is less number of transistor, increased speed, reduced power consumption (Morgenshtein *et al.*, 2002, 2004). Wide range of complex digital function can be implemented by using two transistors in GDI approach. As transistor count decreases overall design area reduces. Improved logic swing and better static power characteristics can be achieved from GDI technique.

The basic two transistor GDI cell is shown in Fig. 2. At first look, the GDI cell brings back to the standard inverter cell design but, there exist some remarkable differences. Three inputs of GDI cell are N, P and G:
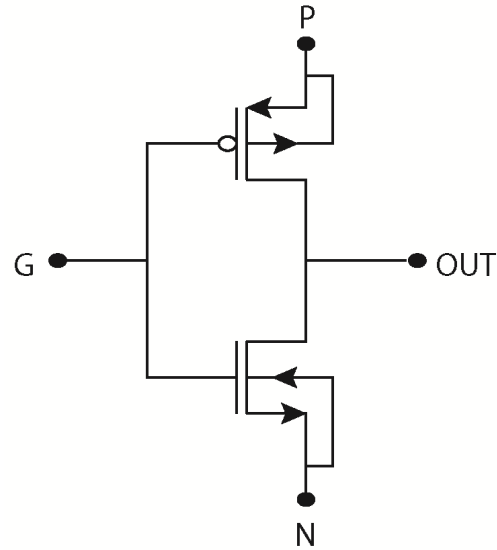

Fig. 2: Basic GDI cell

- N; input data applied to drain/source of NMOS transistor
- p; input data applied to source/drain of PMOS transistor
- G; input data applied to common gate of NMOS and PMOS transistor

Bulk terminal of both NMOS and PMOS is arbitrarily biased by connecting, it with N and P terminals, respectively. The main practical limitation of GDI technique is swing degradation and high complexity in fabrication process; it cannot be fabricated by using standard CMOS process because of direct bulk connection to input pins N and P. As supply voltage to PMOS and ground to NMOS is not fixed in this technique, low voltage swing problem occurs which will affect the implementation of analog circuits. The voltage swing is due to threshold drops which results in performance degradation and increased Short Circuit (SC) power. Since, transistor count of GDI is less than that of standard logic styles, significant drop in overall power was observed.

The four port GDI cell works as new multi-functional device. By applying different data signals to the input ports N, P and G six different Boolean functions can be implemented and is shown in Table 1.

The CMOS NAND and NOR gates are usually preferred for the static digital design. The main reason for that is, both NAND and NOR gate can be designed using four transistors and their functions is a universal set. Funct. 1 and 2 are universal set for GDI, compared to NAND and NOR, it consist only two transistors.

Table 1: Boolean functions implemented by using basic GDI cell

N	P	G	Out	Function
0	B	A	A'B	F1
B	1	B	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B'	B	A	A B'+A'B	XOR

Table 2: Boolean functions implemented by using basic GDI cell

A	B	Functionality	F1
0	0	PMOS trans gate	Vtp
0	1	CMOS inverter	1
1	0	NMOS trans gate	0
1	1	CMOS inverter	0

Table 3: Boolean functions implemented by using basic modified GDI cell

N	Sn	P	Sp	G	Out	Functions
0	0	1	1	X	X'	Inverter
X	X	0	X	Y	XY	AND
1	0	X	OUT	Y	X+Y	OR
X'	0	X	1	Y	X'Y+X Y'	XOR
X	0	X'	1	XY+X'Y'	XNOR	
0	0	Y	Y	X	X'Y	Function 1
Y	0	1	1	X	X'+Y	Function 2
Z	0	Y	1	X	X'Y+XZ	MUX

GDI analysis: The main problem related to PTL design is threshold (Vth) drop across single channel pass-transistor as a result of low voltage swing at the output. The problem can be resolved by adding extra buffering circuitry.

Following analysis is carried out to understand the low output voltage swing problem in GDI cell. Analysis is carried out based on F1 function later we can continue with other GDI functions. Table 2 represents all available logic state vs functionality modes of F1 function. From Table 2, when A = 0, B = 0 the low output voltage swing occurs. In this case, output voltage is Vtp because PMOS will not pass pure zero. The effect occurs when voltage level of B changes from VDD to 0.

If we apply B = 1 in function F1 it will works as a full swing inverter and can be used in logic swing restoration application in digital buffers. By using swing restoration transistor, these problem can be eliminated but increase the transistor count but finally, it will reduce static power consumption. These transistor only triggered when voltage drop (threshold drop) occurs at the output (i.e., Vth instead of logic 0 or VDD-Vth instead of logic 1 or VDD).

Modified GDI cell: To overcome the limitation like logic swing degradation and complex fabrication process of basic GDI cells, a new logic style called modified GDI (Balasubramanian and Joh, 2006; Dangeti and Singh, 2012) technique is proposed. This technique allows designers to get reduction in area, transistor count, delay and power
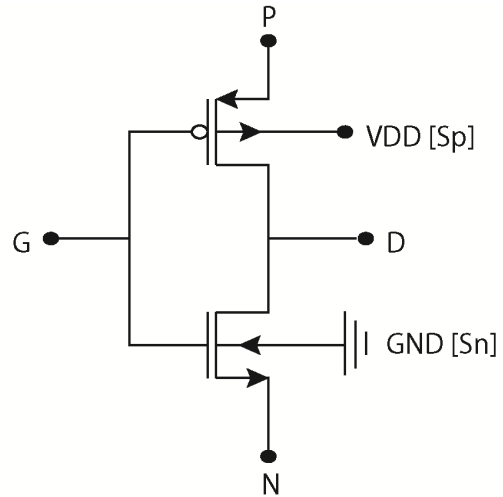

Fig. 3: Basic modified GDI cell

dissipation of digital circuits. Figure 3 represents modified GDI cell, compared to basic GDI cell, mod. GDI cell consists:

- Sp is a low voltage terminal connected to supply voltage (constant high voltage)
- Sn is a high voltage terminal connected to ground (constant low voltage)

Bulk node of PMOS transistor is joined to VDD (supply voltage) and bulk node of NMOS transistor is linked to ground in Modified GDI cell. Now, the basic cell resembles like a standard CMOS inverter (i.e., four terminal PMOS and NMOS). So, it can be easily fabricated by using standard CMOS process. Table 3, represents different input configuration and logic cells implemented using basic mod GDI cells.

Compared to static CMOS design this arrangement have remarkable reduction in both sub-threshold and gate leakage. Compared to basic GDI cell it has improved logic level swing and static power characteristics. Since, the performance of modified GDI cell is testable, it is a favorable new entrance to logic circuit design.

RESULTS AND DISCUSSION

Transistor level power optimization is carried out by GDI technique. The GDI cell is implemented in HSPICE and compared with existing CMOS logic. From Table 4, it is observed that GDI technique consumes 30% whereas TG technique consumes 78% when compared to CMOS AND gate. From Table 5 shows GDI technique consumes 58% whereas TG technique consumes 76% when compared to CMOS OR gate.

From Table 6, it clear that GDI technique consumes 33% whereas TG technique consumes 63.8% when

Table 4: GDI AND gate power analysis

AND gate	GDI technique (w)	Standard CMOS (w)	TG logic (w)
Average power	2.54×10^{-5}	8.6×10^{5}	6.8×10^{-5}
Peak power	8.9×10^{-5}	9.77×10^{-3}	$9.1x10^{3}$

Table 5: GDIXOR gate power analysis

XOR gate	GDI Technique (w)	Standard CMOS (w)	TG logic (w)
Average power	4.65×10^{-5}	7.88×10^{-5}	5.99×10^{-5}
Peak power	4.05×10^{-5}	7.38×10^{-3}	6.6×10^{-3}

Table 6: GDI OR gate power analysis

OR gate	GDI Technique (w)	Standard CMOS (w)	TG logic (w)
Average power	6.2×10^{-5}	18.65×10^{-5}	11.9×10^{-5}
Peak power	6.34×10^{-3}	6.84×10^{-3}	8.2×10^{-3}

Table 7: GDI MUX power analysis

MUX	GDI Technique (w)	Standard CMOS (w)	TG logic (w)
Average power	1.877×10^{-5}	4.58×10^{-5}	6.75×10^{-5}
Peak power	2.98×10^{-4}	3.67×10^{-3}	3.92×10^{-3}

Table 8: GDI 4 bit MAC power analysis

Vedic parallel MAC (4 bit)	GDI technique (w)	Standard CMOS (w)	TG logic (w)
Average power	4.4×10^{-3}	11.2×10^{-3}	11.9×10^{-3}
Peak power	224×10^{-3}	629×10^{-3}	651.7×10^{-3}

Table 9: GDI 8 bit MAC power analysis

Vedic parallel MAC (8 bit)	GDI technique (w)	Standard CMOS (w)	TG logic (w)
Average power	1.2×10^{-2}	3.5×10^{-2}	2.4×10^{-2}
Peak power	812×10^{-3}	2190×10^{-3}	2369×10^{-3}

compared to CMOS XOR gate. From Table 7, researchers can observe that GDI technique consumes 41% whereas TG technique consumes 67.8% when compared to CMOS based MUX. From Table 8 shows that GDI technique consumes 39% whereas TG technique consumes 62.1% when compared to CMOS 4 bit vedic parallel MAC implementation.

From Table 9, it is clear that GDI technique consumes 34.2% whereas TG technique consumes 68.5% when compared to CMOS 8Bit vedic parallel MAC implementation.

CONCLUSION

The Gate Diffusion Input (GDI) based vedic parallel Multiplier Accumulator (MAC) unit is highly efficient in terms of power when compared to parallel MAC unit developed using standard CMOS technique. The proposed architecture is synthesized using 90 nm CMOS library. Average and peak power reports from synopsys HSPICE show that the overall circuit power of proposed design is drastically reduced by using GDI technique.

RECOMMENDATIONS

In future, the GDI optimized MAC unit performance can further be tested in Arithmetic Logic Unit (ALU).

Moreover, the MAC architecture can be effectively used in filters, image processing, digital signal processing applications, etc.

REFERENCES

Aliparast, P., Z.D. Koozehkanani, A.M. Khiavi, G. Karimian and H.B. Bahar, 2011. A very high-speed CMOS 4-2 compressor using fully differential current-mode circuit techniques. Analog Integr. Circuits Signal Process., 66: 235-243.

Balasubramanian, P. and J. Joh, 2006. Low power digital design using modified GDI method. Proceedings of the International Conference on Design and Test of Integrated Systems in Nanoscale Technology (DTIS.), September 5-7, 2006, IEEE, New York, USA., pp: 190-193.

Chang, C.H., J. Gu and M. Zhang, 2004. Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits. IEEE. Trans. Circuits Syst. Regular Papers, 51: 1985-1997.

Dangeti, M. and S.N. Singh, 2012. Minimization of transistor count and power in an embedded system using gdi technique. Universal J. Appl. Comput. Sci. Technol., 2: 308-313.

Huddar, S.R., S.R. Rupanagudi, M. Kalpana and S. Mohan, 2013. Novel high speed vedic mathematics multiplier using compressors. Proceedings of the International Multi-Conference on Automation Computing Communication Control and Compressed Sensing (iMac4s), March 22-23, 2013, IEEE, New York, USA., ISBN:978-1-4673-5089-1, pp: 465-469.

Jithin, S. and E. Prabhu, 2015. Parallel multiplier-accumulator unit based on vedic mathematics. ARPN. J. Eng. Appl. Sci., 10: 3608-3613.

Morgenshtein, A., A. Fish and I.A. Wagner, 2002. Gate-Diffusion Input (GDI): A power-efficient method for digital combinatorial circuits. IEEE Trans. Very Large Scale Integr. Syst., 10: 566-581.

Morgenshtein, A., A. Fish and I.A. Wagner, 2004. An efficient implementation of D-Flip-Flop using the GDI technique. Proceedings of the 2004 International Symposium on Circuits and Systems (ISCAS'04), May 23-26, 2004, IEEE, New York, USA., ISBN:0-7803-8251-X, pp: 672-673.

Seo, Y.H. and D.W. Kim, 2010. A new VLSI architecture of parallel multiplier-accumulator based on Radix-2 modified booth algorithm. IEEE. Trans. Very Large Scale Integr. (VLSI.) Syst., 18: 201-208.

Tirthaji, S.B.K., 1986. Vedic Mathematics or Sixteen Simple Sutras from the Vedas. Motilal Banarsidas Publisher, Varanasi, India.