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An Efficient 1-Bit Full Subtractor Circuit Using Hybrid CMOS Logic

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Abstract: The 1-bit full subtractor circuit plays the vital role in the design of arithmetic circuits. Full adder also acts as full subtractor when, we change all the inputs to complemented but here, we created a new low power single bit 8T full subtractor circuit where the only subtractor is needed. There are three parts used to design the full subtractor. That are passtransistor logic, 2T multiplexer and 3T XOR. It is a hardware efficient full subtractor circuit with a minimum number of MOS transistor counts that reduces the cruel problem of power. It also naturally reduces the delay of the overall circuit. The expexted simulation result of the proposed circuit has less power, the small size of chip area and high speed compared to 14, 15 and 16T full subtractor. The simulation result has been taken from Microwind 3.5 EDA tool on BSIM4 (advanced) 65nm technology at 0.7v supply voltage.

Key words: Full subtractor, low power, PTL, CMOS VLSI, multiplexer, XOR

INTRODUCTION

In CMOS VLSI design the power is a major considerable factor. In recently, advanced applications are require most complexity and a significant number of transistors in the circuit. So, the power consumption and the circuit area are growing as well. The high power and large area of the ICs are helped to increase temperature and also it openly reduces the charge of the power storage in portable devices. The complexity and a large number of transistor count have produced the temperature on circuit run time and it severely affects circuit operation (Chandrakasan *et al*., 1992).

Full subtractor is used the Arithmetic Logic Unit (ALU) and also it is a fundamental unit circuit used for image processing application, Analog-to-digital and digital-to-analog converter (Weste and Eshraghian, 1993). In video coding for wireless surveillance applications, the real-time background subtractor is used to sense any motion activity in the present image. Therefore, reducing power and area in full subtracter will reduce the overall power and area of the whole system.

The full adders circuits are a vital component in all electronics application. It needs to consider of parameters like power, chip size, worst case delay, the temperature in running condition and good driving ability (Bui *et al*., 2000). But, dedicated subtractor units are required in some Digital Signal Processing (DSP) applications. In this study, we consider about power consumption area and delay of the full subtractor.

CONVENTIONAL 1-BIT FULL SUBTRACTOR

The conventional subtractor has been designed by original equations given as:

$$Diff = A\hat{}B\hat{}C;\ Borrow = A'B+BC+A'C$$

It was designed by using two XOR gates, three AND gates, one OR and one inverter gate (Fig. 1). The binary values of A, B and C are inputs of the full subtractor. It has eight different combinations to be used as inputs. Then, the output difference and borrow took from that circuit. It is a digital circuit that used by only zeros and ones. It is designed by transistor level. The transistor

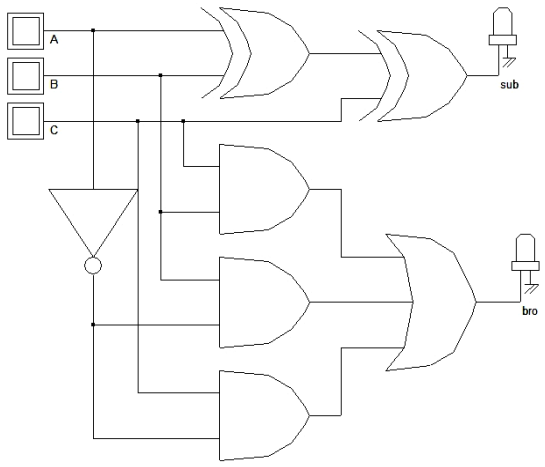

Fig. 1: Conventional 1-bit full subtractor

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level circuit can be implemented by CMOS logic or pass transistor logic. But, transistor count of both CMOS and Pass transistor logic is much high.

CMOS logic is based both nMOS and pMOS transistor and it has complementary outputs (Weste and Eshraghian, 1993). In this concept, number of the transistor of nMOS and pMOS must equal, so the number of total transistors is increasing power compare to other logic. The speed of CMOS logic is better than other logic.

MATERIALS AND METHODS

Modified 1-bit full subtractor: Figure 2 shows that new modified structure of 1-bit full subtractor. It is designed by using the multiplexer and other essential gates. Table 1 shows truth table of 1-bit full subtractor. It has eight combinations of inputs. It is a digital circuit, so it deals with only zeros and ones. The input of modified 1-bit full subtractor is A, B and C. Here, A is a Most Significant Bit (MSB) and C is Least Significant Bit (LSB).

MSB is given to the input of multiplexer and LSB is given to all other gates. The input A is zero in first four combinations of the inputs of the full subtractor and second four combinations are one. So that the A value used as a select signal of two multiplexers. Then, the difference output of the full subtractor is equal to the XOR and XNOR gate's output which has an input of B, C. The borrow output of the full subtractor is similar to the OR and AND gate's output which has input of B, C. So, here, the basis gates XOR, XNOR, OR and AND are introduced. The transistor level circuit can be designed by using 2T multiplexer, 3T XOR, PTL.

2T multiplexer: The multiplexer is designed by two transistor one is pMOS another one is nMOS (Fig. 3). It has no direct supply voltage. So, it reduces much amount of leakage current of the multiplexer circuit (Sharma *et al*., 2010). Both gate terminals of transistors connected to select signal of the multiplexer. The source of nMOS and pMOS transistor is connected to input signal A, B and drain of this transistor are connected to the multiplexer output.

3T XOR: Figure 4 shows that single bit XOR gate using three MOS transistors. The full subtractor difference equation have tow XOR gate. So, the XOR gate is an essential block. The connection changed CMOS inverter and pMOS pass transistor is used to design 3T XOR gate (Bui *et al*., 2000). The 3T XOR have two pMOS and one nMOS transistor. The inputs A is given to the gate of one pMOS and nMOS, the source of another pMOS. Then,

Table 1: The 1-bit full subtractor truth table

A	B	C	DIFF	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

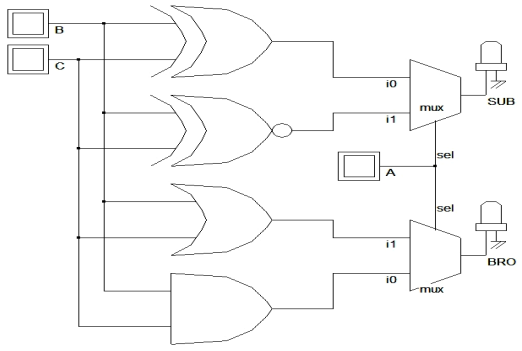

Fig. 2: Modified 1-bit full subtractor

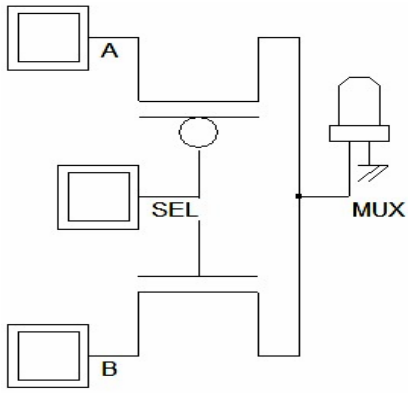

Fig. 3: The 2T multiplexer

the B input is given to the source of first pMOS and the gate of the second pMOS. The output of the 3T XOR gate is taken from the drain of all transistors (Wang *et al*., 1994; Vigneswaran *et al*., 2006). The source is connected to the ground. It also has no supply voltage or Vdd. So, it can reduce the leakage current of the XOR gate.

Pass Transistor Logic (PTL): Compare to CMOS logic PTL is designed by less number transistor. So, power and area are optimized in PTL circuit. It has no connection to supply voltage and ground so, it has less amount leakage current. Inputs can be given in all three terminals and outputs can be taken from both source and drain. Mostly nMOS PTL used in pass transistor logic. PTL can design universal gates and basic gates (Bui *et al*., 2002).

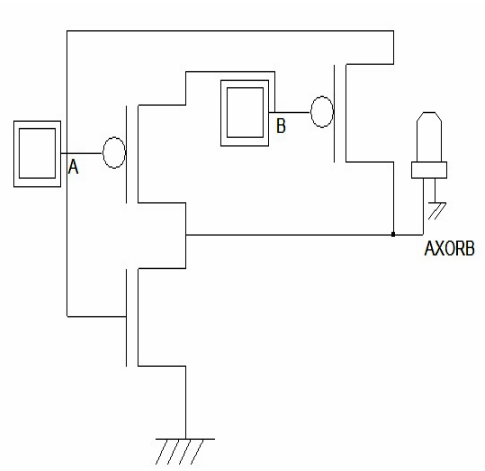

Fig. 4: The 3T XOR

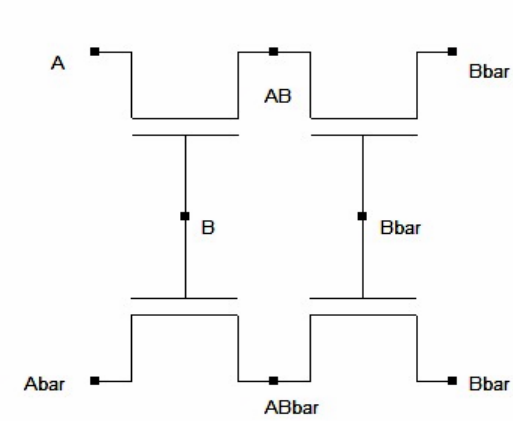

Fig. 5: The PTL AND and NAND

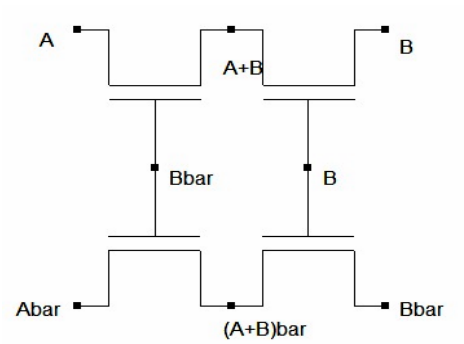

Fig. 6: The PTL OR and NOR

Figure 5 shows that PTL AND and NAND gate. The inputs of PTL are some of them inverter. The circuit is designed by designer's application. The output of the circuit is zero or one so that it is designed for the particular application. Figure 6 and 7 shows PTL OR, NOR, XOR and XNOR.

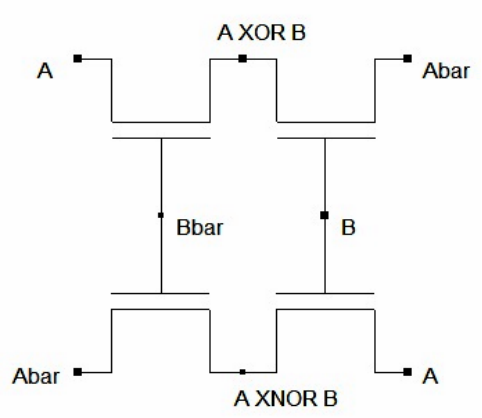

Fig. 7: The PTL XOR and XNOR

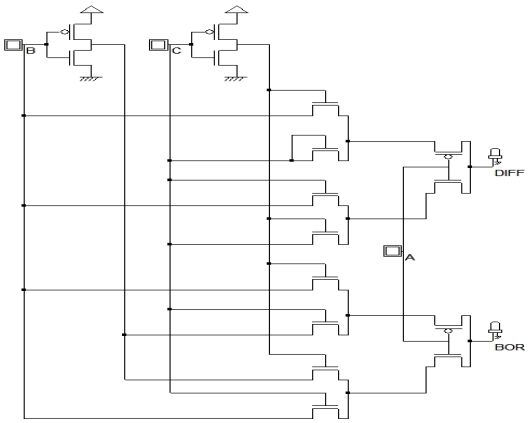

Fig. 8: The 16T 1-bit full subtractor

16T 1-bit full subtractor: Figure 8 shows that 16T 1-bit full subtractor. Basic inverter, PTL and 2T multiplexer used to design this circuit (Bui *et al*., 2002).

15T 1-bit full subtractor: Pass transistor logic XOR and XNOR replaced by 3T XOR and inverter gate from 16T 1-bit full subtractor shown in Fig. 9 (Sharma *et al*., 2010).

14T 1-bit full subtractor: The pass transistor logic-XOR circuit is replaced by two 3T XOR circuit from 16T 1-bit full subtractor (Fig. 10). The difference output of 1-bit full subtractor is design by using six transistors. The borrow output of the subtractor is design by using eight transistors (Sharma *et al*., 2010).

8T 1-bit full subtractor: The design of 8T full subtractor has two 3T XOR gate circuit and one multiplexer (Fig. 11-13). In hybrid CMOS logic 8T full subtractor is used very least number of the transistor.

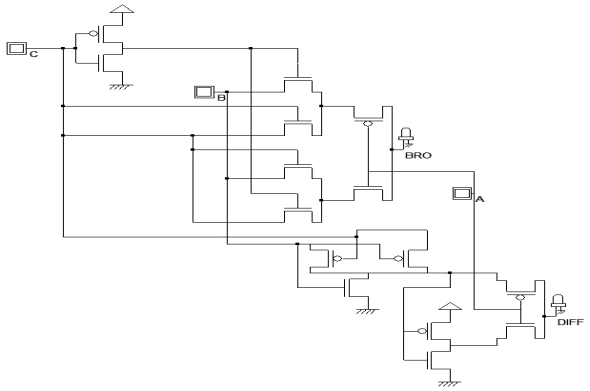

Fig. 9: The 15T 1-bit full subtractor

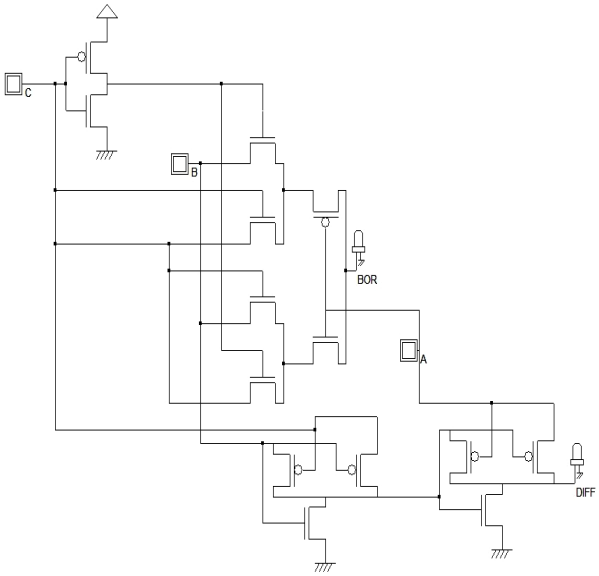

Fig. 10: The 14T 1-bit full subtractor

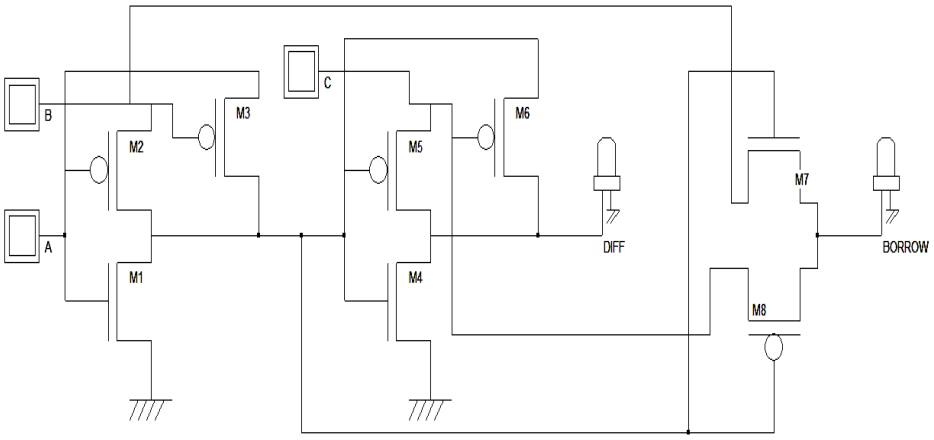

Fig. 11: The 8T 1-bit full subtractor

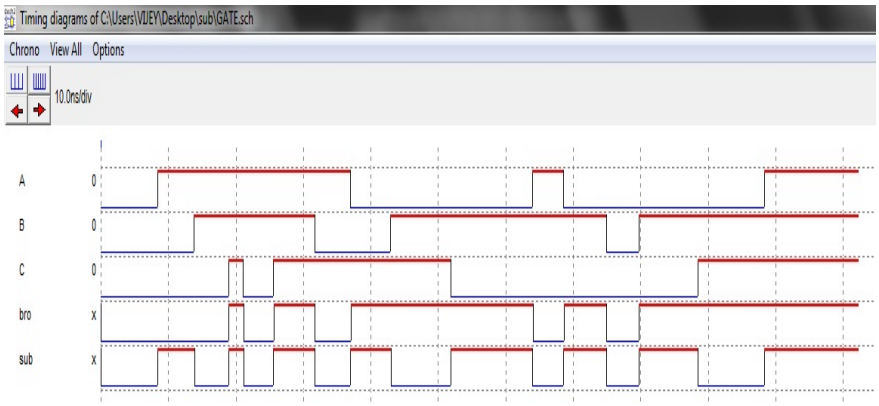

Fig. 12: The 8T 1-bit full subtractorpulse waveform

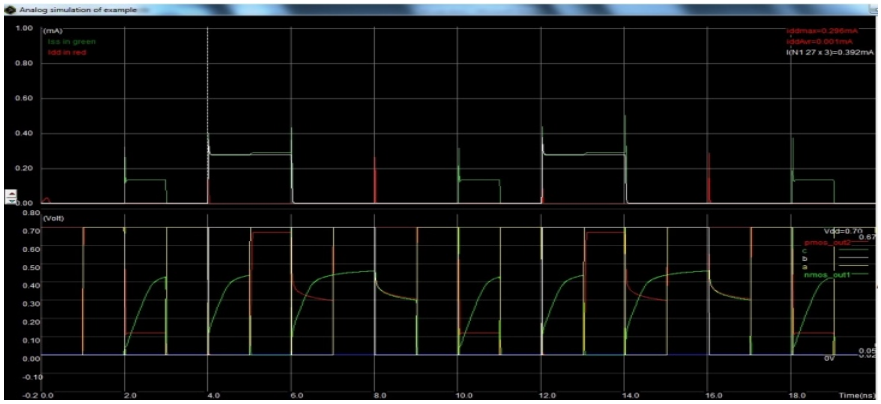

Fig. 13: The 8T 1-bit full subtractor V-I characteristics

RESULTS AND DISCUSSION

The simulation environmental set up made by VLSI back-end EDA tool Microwind 3.5 and DSCH 3.5. The supply voltage ranges varying depends on the technology file of the EDA tool in 65nm technology supply voltage ranges from 0.7-2.5v (MICRWIND, 2011). The efficient performance of the full subtractor circuit is calculated by giving the same inputs to 8T full subtractor and another various count transistor full subtractor. Comparative analyses on the different subtractor 16, 15 and 14T have been done using 65 nm technology. In our proposed 8T subtractor circuit, we have reduced the aspect ratio of the number of transistors and as a result, it gives the best performance compared to any other circuit.

The simulation result, the power consumption of 8T full subtractor is 84.3% better than the 16T full subtractor. Similarly, the are of the chip in 65 nm technology; 8T full subtractor is 51.6% and worst case delay of the 8T full subtractor is 61.7% better than the 16T full subtractor.

Table 2: Performances and analysis

Transistor count	Power (µw)	Area (nm^2)	Delay (fs)
16T	3.95	0.188	0.339
15T	2.95	0.170	0.317
14T	1.87	0.161	0.312
8T	0.62	0.091	0.130

Table 2 demonstrates the comparison of another subtractor. The results of the simulations expose that our proposed 1-bit full subtractor cell is proven to be the best then its peer designs if the design aspects are a delay, power consumed and optimized area.

CONCLUSION

The new proposed full subtractor is using 8T which achieves the least area and the smallest amount of power with the lowest transistor count. It is used to design a dedicated full subtractor circuit where the only subtractor is needed. When we use the adder as a subtractor, the complement operation is requiring. That time the bulk

number of the transistor is reduced. So, the image and video application, the vast number of bits input circuit achieve very less amount of power dissipation.

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